Design of a Direct Downconversion Receiver for IEEE802.11a WLAN

by

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B.S.(Physics) (The University of Science and Technology of China) 1994

Thesis submitted for the degree of

Doctor of Philosophy

in

Department of Electrical and Electronic Engineering,
School of Engineering,
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University of Adelaide, Australia

2007

Typeset in LaTeX 2_ε
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Abstract

Wireless communication technologies are no longer limited for voice band applications, but have entered the era for multimedia data link. The IEEE802.11 family, which occupies a bandwidth in the multi-mega hertz region with the highest data rate of 54 Mbps, now has become the most widely deployed wireless LAN standards. The rapid adoption of IEEE802.11 for computer wireless networks and their growing popularity in mobile applications highlight the need for a low cost, low power consumption, and monolithic solution.

To meet this challenge, traditional RF techniques, which revolved around the superheterodyne architecture can no longer be used. On the contrary, new receiver frontend architectures need to be developed to satisfy the demand of system level integration. Direct downconversion receivers directly translate the RF spectrum to the baseband by setting the LO frequency equal to the RF. Due to the single frequency translation, expensive and bulky off-chip filters and 50 ohm I/O matching networks at IF are no longer required. Also, the single-stage quadrature mixers further simplify the receiver design and reduce the power dissipation. Subsequent baseband components and ADCs are also possible to be integrated with the RF frontend to achieve a monolithic receiver chip.

Despite the previously mentioned advantages, the implementation of a direct downconversion receiver has its own set of performance challenges. In particular, the performance is plagued by DC offset, flicker noise, linearity and mismatches etc. The main objective of this project is to investigate the feasibility of using direct downconversion architecture for the IEEE802.11a standard, and implement the design in a 0.18 µm CMOS technology.

By approaching the design issue at a theoretic point of view, extensive modeling and simulations based on a SIMULINK IEEE802.11a physical layer theme have been carried

out to evaluate the receiver performance. SER results of the receiver demonstrate that the impairments associated with zero IF can be minimised to an acceptable level. Under the guidance of the system level analysis, the circuit level design of a monolithic direct downconversion receiver has been implemented in a 0.18 µm RF CMOS process, including the building blocks of an LNA, mixer, baseband amplifier and a channel-selection filter. Particularly, a novel LNA design methodology with an improved noise figure and less power consumption has been developed. The mixer conversion gain and phase noise have been analysed by a novel approach. The combination topology of the highpass DC offset removal filter and the baseband amplifier provids the best linearity with a negligible noise figure degradation. Circuit simulations are performed using the foundry provided RF design kit with enhanced noise models to capture the extra noise of passive and deep submicron devices. Circuit level simulations show a qualified receiver frontend for the IEEE802.11a standard.

As data converters are important building blocks in wireless receivers, research on high performance Sigma-Delta modulators is also included. MATLAB based programs have been developed for both the discrete and continuous time transfer function synthesis. A BPSDM chip with variable centre frequencies has been developed to verify the SDM transfer function algorithm and the design methodology. The design of an ultra fast continuous time SDM is particularly focused on for a broadband data conversion. To alleviate the challenge of the comparator speed limit, a novel noise transfer function with a unit clock delay has been synthesised. With such a delayed transfer function, a three-stage comparator can be acheieved that solves the comparator gain and speed tradeoff. The full chip simulation shows an acceptable performance for the IEEE802.11a standard.

Statement of Originality

This work contains no material that has been accepted for the award of any other degree or diploma in any university or other tertiary institution and, to the best of my knowledge and belief, contains no material previously published or written by another person, except where due reference has been made in the text.

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Acknowledgements

First of all, I would like to thank my supervisors Dr. Said Al-Sarawi and Mr. Michael Liebelt for offering me the great opportunity to study in ChipTec. They have provided me the freedom in choosing the research direction, inspiring discussions, and passionate encouragement.

Also I would like to acknowledge Kiet To, Bobby Yao and Tony Sarros for their cooperation in EDA tools setup and helpful discussions on wireless receiver and Sigma-Delta modulator areas.

The last but not the least, I would like to thank my parents and brother for their insistent encouragement. Also my wife Shunhui Xu and son Xinkai Zhu, without their patience, support and trust, it is not possible for me to pursue the fondness for research and design.

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List of Abbreviations

3G	the third generation
ADC	analog-to-digital converter
AGC	automatic gain control
AWGN	additive white Gaussian noise
BER	bit error rate
BiCMOS	bipolar complementary metal oxide semiconductor
BPSDM	bandpass Sigma-Delta modulator
BPSK	binary phase shift keying
BW	bandwidth
C/A band	coarse/acquisition band
CG	common gate
CDMA	code division multiple access
CMFB	common mode feedback
CMOS	complementary metal oxide semiconductor
CRFB	cascade of resonators feedback
CS	common source
CT	continuous time
DAC	digital-to-analog conversion
dB	decibels
DC	direct current
DR	dynamic range
DSSS	direct sequence spread spectrum
DT	discrete time
FDM	frequency division multiplexing

FFT	fast Fourier transform
GPS	global positioning system
GSM	global system for mobile
IEEE	Institute of Electrical and Electronics Engineers
IF	intermediate frequency
IFFT	inverse fast Fourier transform
IIP3	input third-order intercept point
I/O	input, output
I/Q	inphase, quadrature
IRR	image-rejection ratio
ISI	intersymbol interference
ISM	industrial, scientific, and medical
HPF	highpass filter
LAN	local area network
LHP	left half plane
LNA	low noise amplifier
LO	local oscillation
LPF	lowpass filter
LPSDM	lowpass Sigma-Delta modulator
LTI	linear time invariant
Mbps	megabits per second
MOS	metal oxide semiconductor
MOSFET	metal oxide semiconductor field effect transmitter
NF	noise figure
NMOS	N-type metal oxide semiconductor
NRZ	non-return to zero
NTF	noise transfer function
OFDM	orthogonal frequency division multiplexing
OOBG	out-of-band gain
OSR	oversampling ratio
OTA	operational transconductance amplifier
OTA-C	operational transconductance amplifier, capacitor

OTA-R	operational transconductance amplifier, resistor
P band	precise band
PC	personal computer
PDF	probability density function
PHY	physical
PMOS	P-type metal oxide semiconductor
PN	P-type, N-type
PSD	power spectral density
QAM	quadrature amplitude modulation
QPSK	quadrature phase shift keying
RC	resistor capacitor
RF	radio frequency
RHP	right half plane
RSA	regenerative sense amplifier
RZ	return to zero
SAW	surface acoustic wave
SCL	source coupled logic
SDM	Sigma-Delta modulator
SER	symbol error rate
Si	silicon
SiGe	silicon germanium
SiO2	silicon dioxide
SNR	signal-to-noise ratio
SOC	system on chip
SPICE	simulation program with integrated circuit emphasis
STF	signal transfer function
TF	transfer function
TSMC	Taiwan semiconductor manufacturing company
U-NII	unlicensed national information infrastructure
VCCS	voltage controlled current source
VCF	variable centre frequency
VGA	variable gain amplifier

WCDMA	wideband code division multiple access
WLAN	wireless local area network
ZPK	zero, pole, gain