Design of a Direct Downconversion Receiver for IEEE802.11a WLAN

by

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B.S.(Physics) (The University of Science and Technology of China) 1994

Thesis submitted for the degree of

Doctor of Philosophy

in

Department of Electrical and Electronic Engineering,
School of Engineering,
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University of Adelaide, Australia

2007

Typeset in LaTeX 2_ε
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Abstract

Wireless communication technologies are no longer limited for voice band applications, but have entered the era for multimedia data link. The IEEE802.11 family, which occupies a bandwidth in the multi-mega hertz region with the highest data rate of 54 Mbps, now has become the most widely deployed wireless LAN standards. The rapid adoption of IEEE802.11 for computer wireless networks and their growing popularity in mobile applications highlight the need for a low cost, low power consumption, and monolithic solution.

To meet this challenge, traditional RF techniques, which revolved around the superheterodyne architecture can no longer be used. On the contrary, new receiver frontend architectures need to be developed to satisfy the demand of system level integration. Direct downconversion receivers directly translate the RF spectrum to the baseband by setting the LO frequency equal to the RF. Due to the single frequency translation, expensive and bulky off-chip filters and 50 ohm I/O matching networks at IF are no longer required. Also, the single-stage quadrature mixers further simplify the receiver design and reduce the power dissipation. Subsequent baseband components and ADCs are also possible to be integrated with the RF frontend to achieve a monolithic receiver chip.

Despite the previously mentioned advantages, the implementation of a direct downconversion receiver has its own set of performance challenges. In particular, the performance is plagued by DC offset, flicker noise, linearity and mismatches etc. The main objective of this project is to investigate the feasibility of using direct downconversion architecture for the IEEE802.11a standard, and implement the design in a 0.18 µm CMOS technology.

By approaching the design issue at a theoretic point of view, extensive modeling and simulations based on a SIMULINK IEEE802.11a physical layer theme have been carried

out to evaluate the receiver performance. SER results of the receiver demonstrate that the impairments associated with zero IF can be minimised to an acceptable level. Under the guidance of the system level analysis, the circuit level design of a monolithic direct downconversion receiver has been implemented in a 0.18 µm RF CMOS process, including the building blocks of an LNA, mixer, baseband amplifier and a channel-selection filter. Particularly, a novel LNA design methodology with an improved noise figure and less power consumption has been developed. The mixer conversion gain and phase noise have been analysed by a novel approach. The combination topology of the highpass DC offset removal filter and the baseband amplifier provids the best linearity with a negligible noise figure degradation. Circuit simulations are performed using the foundry provided RF design kit with enhanced noise models to capture the extra noise of passive and deep submicron devices. Circuit level simulations show a qualified receiver frontend for the IEEE802.11a standard.

As data converters are important building blocks in wireless receivers, research on high performance Sigma-Delta modulators is also included. MATLAB based programs have been developed for both the discrete and continuous time transfer function synthesis. A BPSDM chip with variable centre frequencies has been developed to verify the SDM transfer function algorithm and the design methodology. The design of an ultra fast continuous time SDM is particularly focused on for a broadband data conversion. To alleviate the challenge of the comparator speed limit, a novel noise transfer function with a unit clock delay has been synthesised. With such a delayed transfer function, a three-stage comparator can be acheieved that solves the comparator gain and speed tradeoff. The full chip simulation shows an acceptable performance for the IEEE802.11a standard.

Statement of Originality

This work contains no material that has been accepted for the award of any other degree or diploma in any university or other tertiary institution and, to the best of my knowledge and belief, contains no material previously published or written by another person, except where due reference has been made in the text.

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Acknowledgements

First of all, I would like to thank my supervisors Dr. Said Al-Sarawi and Mr. Michael Liebelt for offering me the great opportunity to study in ChipTec. They have provided me the freedom in choosing the research direction, inspiring discussions, and passionate encouragement.

Also I would like to acknowledge Kiet To, Bobby Yao and Tony Sarros for their cooperation in EDA tools setup and helpful discussions on wireless receiver and Sigma-Delta modulator areas.

The last but not the least, I would like to thank my parents and brother for their insistent encouragement. Also my wife Shunhui Xu and son Xinkai Zhu, without their patience, support and trust, it is not possible for me to pursue the fondness for research and design.

Yingbo Zhu

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List of Abbreviations

3G	the third generation
ADC	analog-to-digital converter
AGC	automatic gain control
AWGN	additive white Gaussian noise
BER	bit error rate
BiCMOS	bipolar complementary metal oxide semiconductor
BPSDM	bandpass Sigma-Delta modulator
BPSK	binary phase shift keying
BW	bandwidth
C/A band	coarse/acquisition band
CG	common gate
CDMA	code division multiple access
CMFB	common mode feedback
CMOS	complementary metal oxide semiconductor
CRFB	cascade of resonators feedback
CS	common source
CT	continuous time
DAC	digital-to-analog conversion
dB	decibels
DC	direct current
DR	dynamic range
DSSS	direct sequence spread spectrum
DT	discrete time
FDM	frequency division multiplexing

FFT	fast Fourier transform
GPS	global positioning system
GSM	global system for mobile
IEEE	Institute of Electrical and Electronics Engineers
IF	intermediate frequency
IFFT	inverse fast Fourier transform
IIP3	input third-order intercept point
I/O	input, output
I/Q	inphase, quadrature
IRR	image-rejection ratio
ISI	intersymbol interference
ISM	industrial, scientific, and medical
HPF	highpass filter
LAN	local area network
LHP	left half plane
LNA	low noise amplifier
LO	local oscillation
LPF	lowpass filter
LPSDM	lowpass Sigma-Delta modulator
LTI	linear time invariant
Mbps	megabits per second
MOS	metal oxide semiconductor
MOSFET	metal oxide semiconductor field effect transmitter
NF	noise figure
NMOS	N-type metal oxide semiconductor
NRZ	non-return to zero
NTF	noise transfer function
OFDM	orthogonal frequency division multiplexing
OOBG	out-of-band gain
OSR	oversampling ratio
OTA	operational transconductance amplifier
OTA-C	operational transconductance amplifier, capacitor

OTA-R	operational transconductance amplifier, resistor
P band	precise band
PC	personal computer
PDF	probability density function
PHY	physical
PMOS	P-type metal oxide semiconductor
PN	P-type, N-type
PSD	power spectral density
QAM	quadrature amplitude modulation
QPSK	quadrature phase shift keying
RC	resistor capacitor
RF	radio frequency
RHP	right half plane
RSA	regenerative sense amplifier
RZ	return to zero
SAW	surface acoustic wave
SCL	source coupled logic
SDM	Sigma-Delta modulator
SER	symbol error rate
Si	silicon
SiGe	silicon germanium
SiO2	silicon dioxide
SNR	signal-to-noise ratio
SOC	system on chip
SPICE	simulation program with integrated circuit emphasis
STF	signal transfer function
TF	transfer function
TSMC	Taiwan semiconductor manufacturing company
U-NII	unlicensed national information infrastructure
VCCS	voltage controlled current source
VCF	variable centre frequency
VGA	variable gain amplifier

WCDMA	wideband code division multiple access
WLAN	wireless local area network
ZPK	zero, pole, gain

Chapter 1

Introduction

1.1 Motivation

The growing demand for wireless connectivity is not only focused on voice-based cellular services, but also expanded to data transmissions, such as WLAN. The emerging of wireless technique for LAN application enables a convenient and fast access to the network for a client anywhere within the range of a base station.

After working for nearly a decade, the IEEE ratified wireless networking communication standards. IEEE802.11b, located at 2.4 GHz ISM frequency band, utilising DSSS modulation, is the first standard for commercial product development. As shown in Figure 1.1, this frequency band is shared with many other systems, therefore interference might occur, limiting the modulation efficiency, and hence data rate.

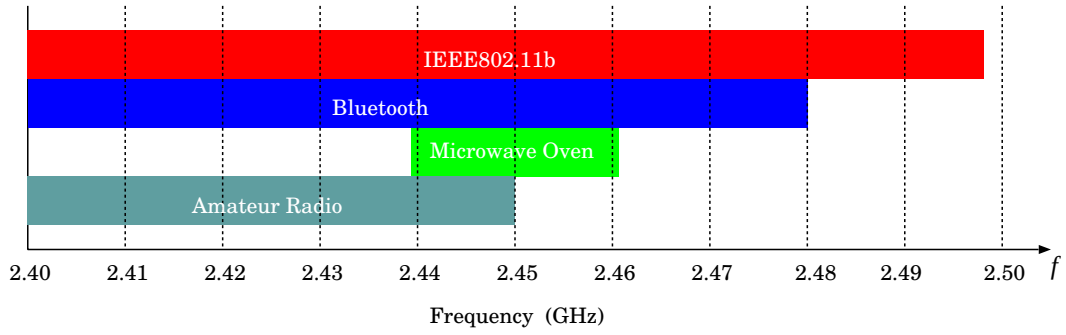

Figure 1.1. Spectrum allocation at 2.4 GHz ISM band

IEEE802.11a standard, revised for high quality network access, specifies operation in the 5 GHz U-NII band. As illustrated in Figure 1.2, there is a contiguous 200 MHz band from 5.15 to 5.35 GHz and a separate 100 MHz band from 5.725 to 5.825 GHz. The lower and middle U-NII bands contain 4 carriers each, with maximum power outputs of 40 mW and 200 mW respectively for indoor WLAN applications. The upper U-NII band contains 4 carries with a maximum power output of 800 mW, intended for outdoor communications.

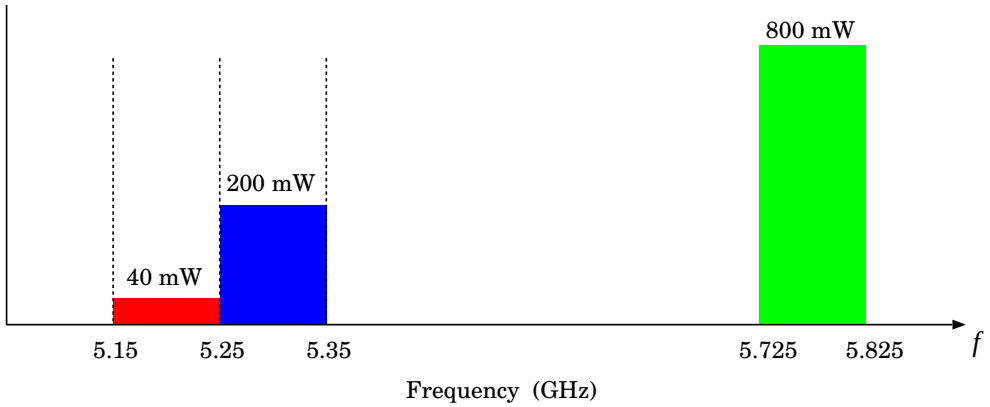

Figure 1.2. Spectrum allocation at 5 GHz band

In the relatively "clean" 5 GHz band, unlike IEEE802.11b, IEEE802.11a employs OFDM technique in order to achieve more efficient spectrum utilisation. Each carrier is further divided into 52 sub-carriers with 312.5 kHz bandwidth transmitted in parallel, among which 48 sub-carriers are used for data. BPSK, QPSK, 16-QAM and 64-QAM modulations can be applied for each sub-carrier yielding the highest data rate of 54 Mbps, which is about 5 times higher than the IEEE802.11b standard. Faster data transmission is perhaps the most attractive reason for both the academic and industry research to focus on the development of IEEE802.11a WLAN devices. The PHY level specifications and data rate for the IEEE802.11a are listed in Table 1.1 and Table 1.2.

RF Frequency	5G ISM Band
Occupied Bandwidth	16.6 MHz
Sub-carrier Interval	312.5 kHz
Noise Figure	$<$ 8.5 dB (30 dB SNR)

Table 1.1. IEEE802.11a PHY specification summary.

Data Rate(Mbit/s)	Min Sensitivity (dBm)	Adj Ch Rejection (dB)
6,9 (BPSK)	-82, -81	16, 15
12, 18 (QPSK)	-79, -77	13, 11
24, 36 (QAM16)	-74, -70	8, 4
48, 54 (QAM64)	-66, -65	0, -1

Table 1.2. IEEE802.11a data rate Vs. receiver sensitivity and adjacent channel rejection.

As long as the development of modern communication specifications, different wireless transceiver architectures are also under extensive investigations. Heterodyne architecture is the most widely used in today's wireless receivers, which translates the RF signal to an IF and then further downconverts the IF to the baseband. The received signal is amplified and bandpass filtered at both the RF and IF stages, resulting in a robust downconverted baseband signal. However, in a heterodyne receiver, the trade-off between image-rejection and channel-selection is a principle problem. The intermediate frequency must be chosen carefully according to the carrier frequency and the performance of the RF and IF bandpass filters. Bandpass filters at the RF and IF are not possible for integration using today's silicon technology. Therefore, external expensive and bulky filters have to be employed. The impedance matching network at the RF and IF I/O ports and the two downconversion mixers increase the receiver power dissipation and design complexity.

Numerous efforts have been put on homodyne (also named zero-IF or direct downconversion) architecture recently in the research area. A homodyne receiver directly downconverts the incoming RF signal to the baseband by setting the mixer LO frequency equal to the RF, hence the image problem is vanished. The channel is selected at the baseband by an on-chip lowpass filter. Since no external IF filters are required, a monolithic receiver chipset is achievable with lower power consumption and comparatively simple circuitry design. The industry also has accepted homodyne architecture and successfully developed commercial product for 3G CDMA and GPS receivers [1]. Despite these advantages, serious difficulties such as the DC offset, flicker noise and even order distortions are appeared when implementing a homodyne receiver. Careful evaluation of those impairments related to the direct downconversion is necessary.

The aim of this project is to investigate the possibility of using direct downconversion architecture for the IEEE802.11a standard and implement the design in a 0.18 µm CMOS

process. The research focuses on the low power, low noise figure, and high linearity receiver design for mobile applications.

As data converters are important building blocks in wireless receivers, research on high performance Sigma-Delta modulators is also included. MATLAB based programs have been developed for both the discrete and continuous time transfer function synthesis. The design of an ultra fast continuous time SDM is particularly focused on for a broadband data conversion.

The major contributions made in this thesis are listed below.

- Provided a systematical analysis of the feasibility of using the direct downconversion architecture for the IEEE802.11a standard wireless receivers.
- Provided a novel LNA design methodology for very low noise figure and high linearity.
- Analysed the Gilbert mixer performance including the conversion gain and the flicker noise issue.
- Demonstrated a HPF-VGA combination topology with good noise performance and linearity.
- Developed a MATLAB program set for the synthesis of different types of SDMs, including DT, CT, LPSDM, BPSDM and VCFBPSDM, etc.
- Developed and tested a VCFBPSDM chip to verify the SDM design methodology and the VCF algorithm.
- Designed a novel 1 GHz second-order LPSDM using TSMC 0.18 µm CMOS process for the broad band analog-to-digital conversion.

1.2 Thesis Organisation

Chapter 2 provides an overview of the heterodyn, low-IF with image-rejection and the homodyne architectures. The advantages and disadvantages of each architecture and the selection guidelines are discussed.

Chapter 3 introduces a system level analysis of an IEEE802.11a direct downconversion receiver, including the OFDM modulation, pulse shaping and the noise effect. The feasibility of using the direct downconversion architecture for the IEEE802.11a standard is demonstrated.

A circuit level receiver design is presented in Chapter 4. The LNA design methodology is first introduced, followed by the mixer conversion gain and flicker noise analysis. The VGA and channel-selection filter design is introduced after the frontend building blocks. TSMC 0.18 µm CMOS process with 1.8V voltage supply is used for the receiver chip development.

Chapter 5 introduces the SDM ADC fundamentals, system level transfer function synthesis, and simulation techniques based on MATLAB and SIMULINK tools. Spectrum analysis issues, such as the spectrum leakage and signal power splatter, are particularly discussed. The BPSDM with a variable centre frequency and the CT SDM synthesis are also introduced.

Chapter 6 presents the design of an ultra fast second-order CT SDM for the baseband analog-to-digital conversion. A delayed transfer function is synthesised for a better quantisation performance at high frequencies. A new integrator with negative transconductance compensation is designed to boost the DC gain and realise the transfer function. Transistor level simulation results and the modulator layout are presented.

Finally, summaries of the presented work and the direction for future work are given.

1.3 Publications

- Zhu, Y., Liebelt, M. and Al-Sarawi, S.F., "Variable center frequency bandpass sigma-delta modulator," Proc. of SPIE on CD-ROM, Int. Symposium on Smart Materials, Nano-, and Micro-Smart Systems 2002, Melbourne, 16-18 December 2002. Disk 1: Vols. 4934-4937;

- Y. Zhu, S. Al-Sarawi and M. Liebelt., "1-GHz 2nd-order lowpass sigma delta modulator in CMOS for wireless receivers," Proc. of SPIE on Microelectronics: Design, Technology and Packaging; 2003, Perth, p.35-46, Vols. 5274;

- Y. Zhu, S. Al-Sarawi and M. Liebelt., "The design of a 2.4 GHz LNA with 0.62 dB noise figure," Accepted by SPIE conference, Sydney, Australia, 2004.
- Y. Zhu, S. Al-Sarawi, C. C. Lim and M. Liebelt., "Fourth-Order Discrete-Time variable centre frequency bandpass Sigma-Delta modulator," IEEE APCCAS, Singapore, 2006.

Chapter 2

Receiver Architectures

2.1 Introduction

The most important component in a wireless system is the receiver, which senses an extremely weak RF signal; downconverts the useful band and provides a baseband signal after amplification and filtration with acceptable quality. The extremely weak incoming RF signal is not by intention, but due to the non-ideal environment through which the RF signal travels, such as multi-path fading and the lossy propagation medium.

In addition to the weakness of the received signal, undesired signals, or so-called interferers in the vicinity of the useful RF band can be significantly stronger than the desired RF signal as illustrated in Figure 2.1. Although, these strong interferers are not located inside the signal band at RF, after downconversion, either a fraction or the distortions of the interferes might be located in the baseband due to the receiver non-idealities, thereby corrupting the desired signal.

The weak incoming RF signal and the strong interferers require the receiver to have high sensitivity and selectivity criteria. With different architectures, the receiver sensitivity and selectivity may have different characteristics. Therefore it is important to understand the trade-offs between the different receiver architectures. This chapter provides an overview of three major architectures including heterodyne, low-IF with image-rejection, and homodyne. The main characteristics of each type are introduced as well as the architecture selection guidelines.

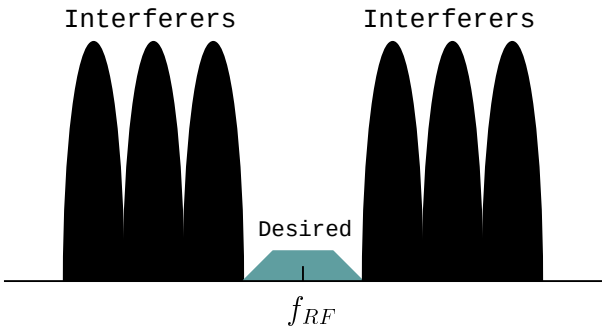

Figure 2.1. RF spectrum with a weak desired signal and strong adjacent interferers.

2.2 Heterodyne

Heterodyne is the most successful architecture on the wireless receiver history and is still widely used today. The incoming signal is bandpass filtered at the RF for image-rejection, and then fed into a downconversion mixer to be translated to an IF. At the IF, the signal passes through a channel-selection filter and then further downconverts to baseband as illustrated in Figure 2.2. Red building blocks in the figure represent off-chip components. Two gain stages and off-chip filters at RF and IF stages introduce good receiver sensitivity and selectivity. However the heterodyne architecture has its native defects, which limit its future evolution.

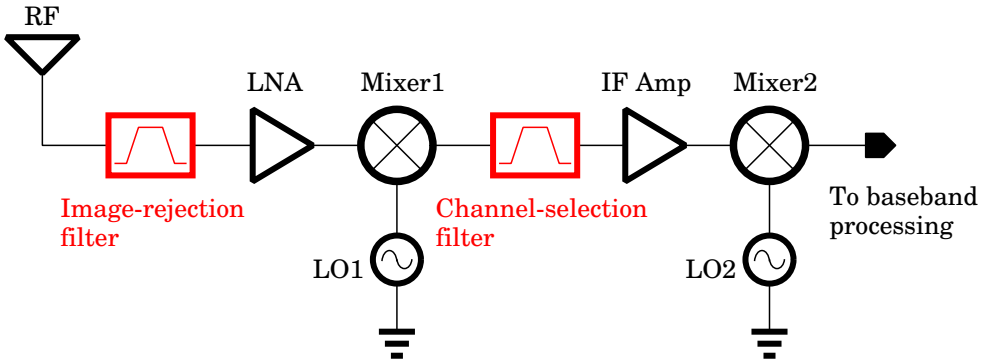

Figure 2.2. Heterodyne architecture.

The image problem arises during the frequency translation in a heterodyne receiver. The RF signal is downconveted to IF by multiplying it by the LO signal, resulting in an IF at $\omega_{LO1} - \omega_{RF}$, where ω_{RF} and ω_{LO1} are the RF and LO frequencies of the first downconversion mixer in radians respectively. However not only ω_{RF} but also $2\omega_{LO1} - \omega_{RF}$, so-called image, is frequency translated to IF, corrupting the downconverted signal of

interest, as illustrated in Figure 2.3(a). Therefore, images must be sufficiently suppressed by an image-rejection filter at RF before downconversion.

In addition to image-rejection, adjacent strong interferers must be attenuated at IF. Although the strong interferers are not directly located in the desired signal band, the third-order distortion, due to the circuitry non-ideal linearity, is possible to enter the band of interest and corrupts the desired signal, as depicted in Figure 2.3(b). Thus a channel-selection filter is applied after the downconversion to IF.

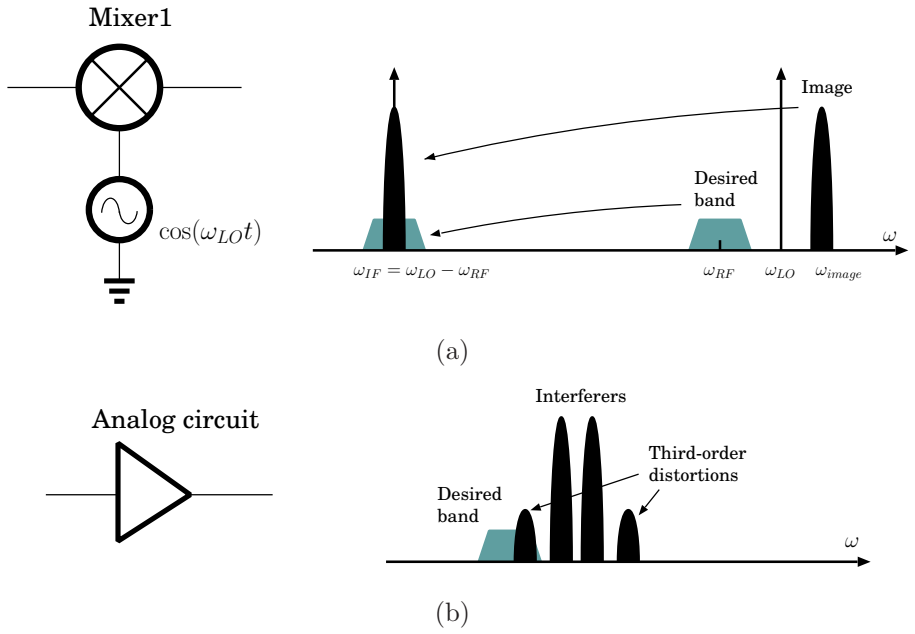

Figure 2.3. (a) Image issue and (b) channel-selection issue in heterodyne receivers.

Filtration with sharp cut-off frequency is very difficult to achieve at high frequencies even with high quality ceramic or SAW filters. In order to provide sufficient attenuation of the image, the LO frequency should be chosen far away from the RF. However, widely split RF and LO frequencies result in a high IF, which challenges the channel-selection filter to sufficiently suppress the adjacent interferers, as illustrated in Figure 2.4(a) [2]. Conversely, for large attenuation of the adjacent interferers, a low IF is required, resulting in poor image-rejection. This is because the LO frequency has to be chosen close to the RF, as depicted in Figure 2.4(b) [2]. The trade-off between image-rejection and channel-selection is a principal issue in heterodyne receivers.

Another trade-off in heterodyne receivers is between the performance and power dissipation. The two amplifiers at the RF and IF do improve the receiver sensitivity

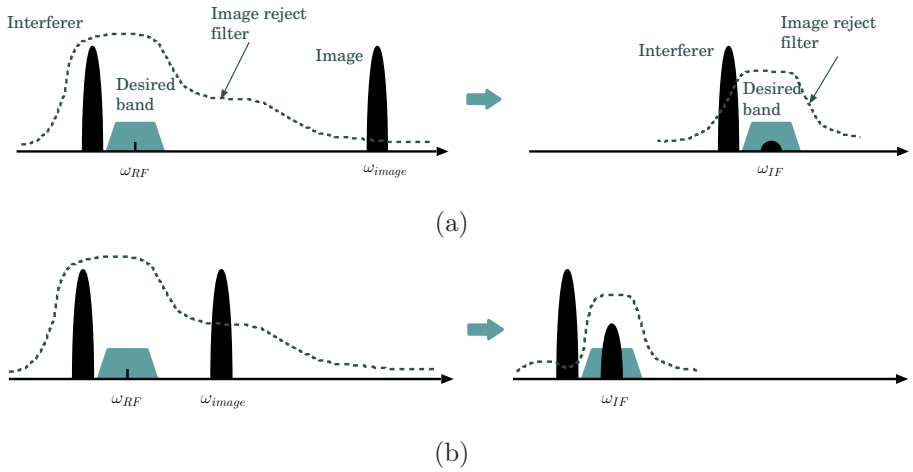

Figure 2.4. Trade-off between image-rejection and channel-selection. (a) High IF issue; (b) low IF issue.

because the desired RF signal is amplified enough to overcome the flicker noise effect at the baseband. However gain stages at high frequencies require large current, hence increase the receiver power dissipation, which is a key issue for a mobile system.

The expensive and bulky off-chip IF filter requires 50 ohm matching networks at the IF I/O interfaces, increasing the receiver design complexity, power consumption, cost and reducing the system integration.

Heterodyne receivers are still widely used in today's wireless systems, especially for narrow bandwidth applications (less than 1 MHz, such as GSM). However, the commercialised applications of heterodyne receivers do not mean the native advantages in this architecture, but a successful compromise to solve the receiver's low frequency non-idealities, which are discussed in Section 2.4.

2.3 Image-Rejection Mixer and Low-IF Architectures

The trade-off between image-rejection and channel-selection can be alleviated by using so-called image-rejection mixers. The mechanism of an image-rejection mixer is to generate two downconverted images with positive and negative polarities; then eliminating the two images by summation. Figure 2.5 shows two possible topologies reported by Hartley and Weaver [3].

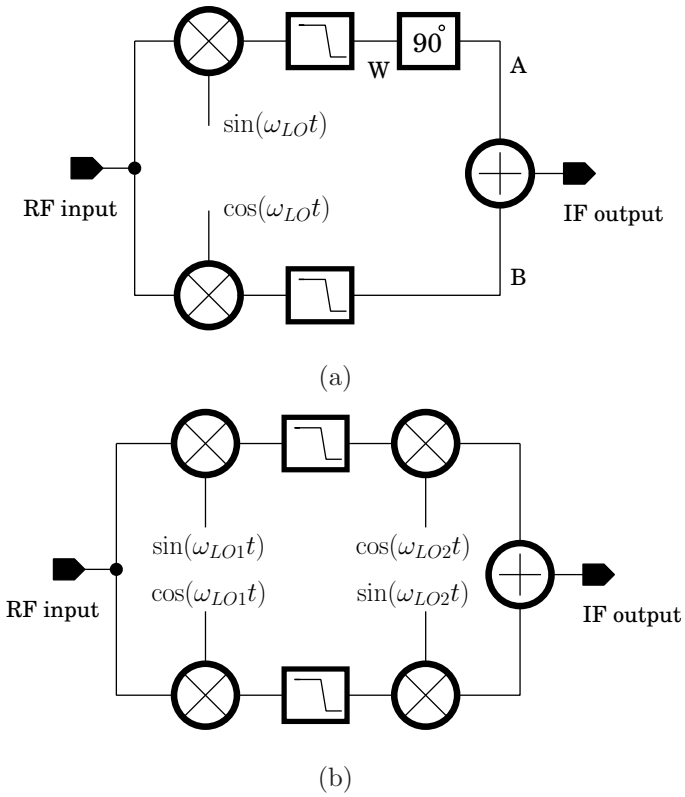

Figure 2.5. Image-rejection architectures. (a) Hartley; (b) Weaver.

In the Hartley topology, assuming the desired input RF signal is $A_{RF}\cos(\omega_{RF}t)$ and the image is $A_{IM}\cos(\omega_{IM}t)$, then the total input is

$$S(t) = A_{RF}\cos(\omega_{RF}t) + A_{IM}\cos(\omega_{IM}t). \tag{2.1}$$

After the quadrature downconversion by multiplying $S(t)$ with $\cos(\omega_{LO}t)$ and $\sin(\omega_{LO}t)$, the signals presented at points W and B are

$$S_W(t) = \frac{A_{RF}}{2}\sin[(\omega_{LO} - \omega_{RF})t] + \frac{A_{IM}}{2}\sin[(\omega_{LO} - \omega_{IM})t], \tag{2.2}$$

$$S_B(t) = \frac{A_{RF}}{2}\cos[(\omega_{LO} - \omega_{RF})t] + \frac{A_{IM}}{2}\cos[(\omega_{LO} - \omega_{IM})t]. \tag{2.3}$$

The high frequency components are neglected due to the lowpass filters after the downconversion. The signal $S_W(t)$ further passes through a shift-by-90° network, which converts sin to -cos and cos to sin respectively, yielding the signal at point A as

$$S_A(t) = \frac{A_{RF}}{2}\cos[(\omega_{LO} - \omega_{RF})t] - \frac{A_{IM}}{2}\cos[(\omega_{LO} - \omega_{IM})t]. \tag{2.4}$$

The total IF output can be obtained by summing $S_A(t)$ and $S_B(t)$ as

$$\begin{aligned} S_{out}(t) &= S_A(t) + S_B(t) \\ &= A_{RF}\cos[(\omega_{LO} - \omega_{RF})t]. \end{aligned} \tag{2.5}$$

The two image related terms are cancelled due to their opposite polarities, resulting in image free.

The Weaver architecture follows the same mechanism. But instead of a shift-by-90° network, a Weaver mixer uses two second-stage mixers to generate downconverted images with different polarities and cancel each other.

The mathematical analysis does give perfect image-rejection. Unfortunately, due to the device mismatch in integrated circuit fabrications, a perfect image-rejection is not possible. The mismatch can result in the two LO phases not being in quadrature, the gains of the two paths not being identical, and the phase shift not being exactly 90°. All these non-idealities introduce incomplete image-rejection. In order to numerically describe the incomplete image-rejection, a term of IRR is defined as the image-to-signal power ratio at the IF divided by that at the RF. For the Hartley architecture, the IRR in dB is given by [2]

$$\text{IRR(dB)} \approx 10\log\left[\frac{\epsilon^2 + \theta^2}{4}\right], \tag{2.6}$$

where ϵ denotes the voltage gain mismatch and θ is the phase error in radians. For the Weaver architecture, the IRR in dB is given by [4]

$$\text{IRR(dB)} \approx 10\log\left[\frac{1 + (1+\Delta A)^2 + 2(1+\Delta A)cos(\Delta\Phi_{LO1} + \Delta\Phi_{LO2})}{1 + (1+\Delta A)^2 + 2(1+\Delta A)cos(\Delta\Phi_{LO1} + \Delta\Phi_{LO2})}\right], \tag{2.7}$$

where ΔA is the gain error and $\Delta\Phi_{LO1}$, $\Delta\Phi_{LO2}$ are the phase errors of the first-stage and the second-stage downconversion mixers respectively. In practise, an IRR is limited to 25∼40 dB due to the mismatch issue, without extra calibration techniques [5].

A low-IF receiver, based on an image-rejection mixer, downconverts the RF to a very low IF to avoid strong non-idealities at low frequencies. As illustrated in Figure 2.6, the low-IF signal is usually digitised after amplification and channel-selection. The further frequency translation to the baseband is performed in the digital domain. To achieve very low IF, a very high LO frequency is required, thereby the RF filter cannot sufficiently attenuates the image. Thus, image-rejection downconversion mixers are necessary for low-IF receivers.

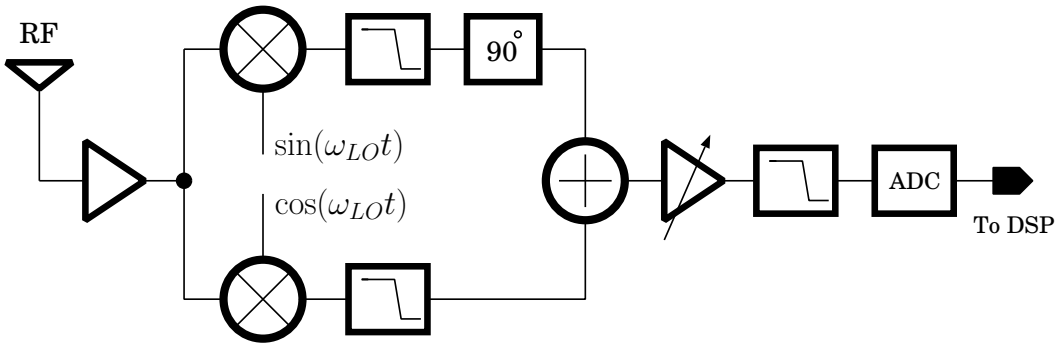

Figure 2.6. Low IF receiver architecture.

Because of the limited IRR, a strong image could be a serious problem for utilising the low-IF architecture. However, for some particular applications, such as GPS C/A band receivers, there are no strong signals in the vicinity of the desired C/A band signal, but only the very weak P band spectrum. As depicted in Figure 2.7, if the LO is chosen to make the image located inside the P band, then the IRR criteria is significantly relaxed.

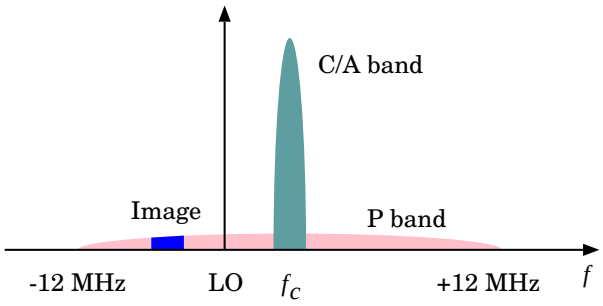

Figure 2.7. GPS C/A band low-IF downconversion with a very weak image inside the P band.

The low-IF architecture eliminates the need for external IF filters, so that monolithic receiver chips are achievable, especially for those applications without strong images. However more complex image-rejection downconversion mixers are necessary and may consumes more power.

2.4 Direct Downconversion Architecture: Chances and Challenges

The trade-off between image-rejection and channel-selection is a principle drawback in heterodyne receivers. Although with the image-rejection mixer architecture, the IRR is limited by the inevitable mismatch in practise. Homodyne receivers, introduced by Colebrook in 1924 [6], directly translate the RF spectrum to the baseband by setting the LO frequency equal to the RF. Therefore, the image is just the RF signal itself, eliminating the image problem. Because of this feature, homodyne receivers are also named as zero-IF or direct downconversion receivers.

The block diagram of a direct downconversion receiver is shown in Figure 2.8. The direct downconversion mixer frequency translates the RF to baseband, therefore the expensive and bulky off-chip filters and 50 ohm I/O matching networks at IF are no longer required. Also the single-stage quadrature mixers further simplifies the receiver design and reduces the power dissipation. The subsequent baseband components and ADCs are also possible to be integrated with the RF frontend to achieve a monolithic receiver chip.

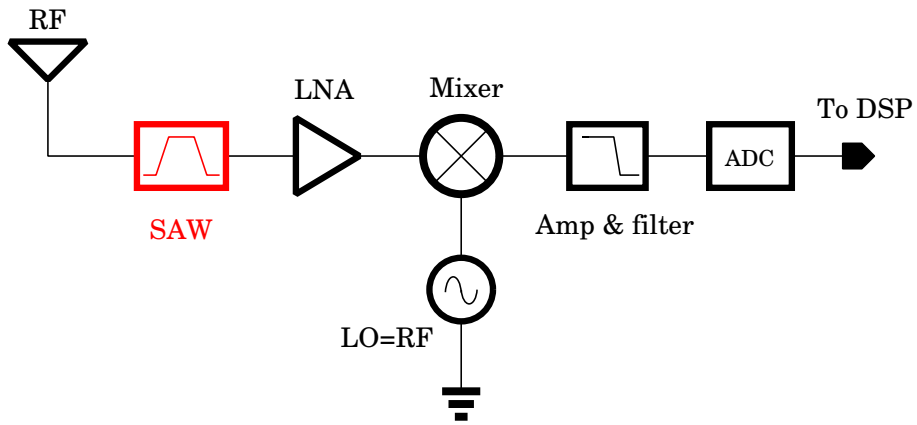

Figure 2.8. Direct downconversion architecture block diagram.

Despite the previously mentioned advantages, the implementation of a direct downconversion has its unique and serious difficulties. There are several issues arising when the LO frequency is approaching the RF as illustrated in Figure 2.9. The most well-known effect in a direct downconversion receiver might be the DC offset. Due to the non-ideal isolation between the LO port and the RF port, the LO signal can leak to the antenna and the LNA. Because the LO frequency is equal to the RF, this leakage is self-mixed

when passing through the mixer and generates the undesired DC component. This DC offset may saturates the subsequent baseband components after amplification and also degrades the receiver SER. In a spread spectrum system, a single beat interferer, such as the DC offset, is less troublesome to reduce the SER, because it appears as a jamming signal and its power will be spread when de-spreading the desired signal spectrum [7].

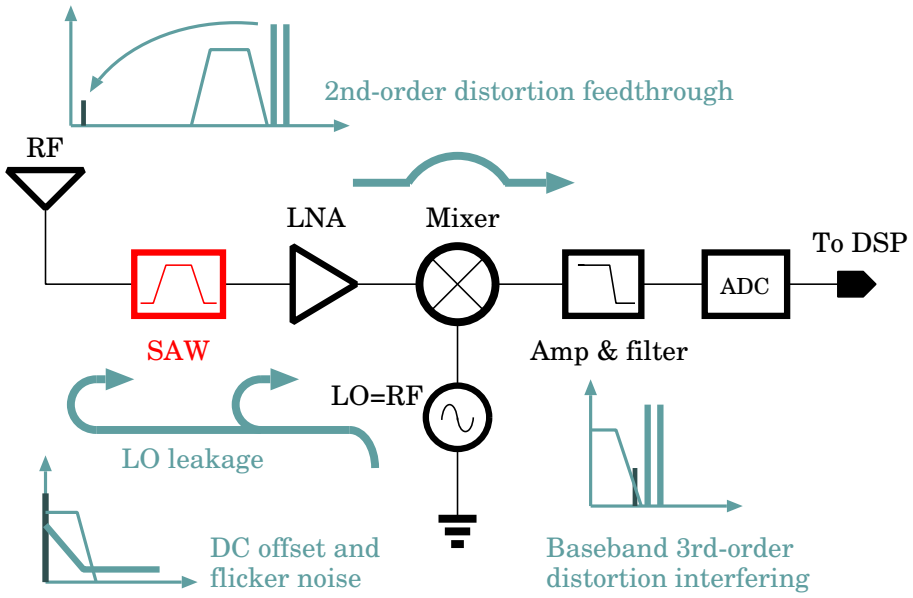

Figure 2.9. Design issues in the direct downconversion architecture.

Flicker noise is another low frequency interference source, which substantially corrupts the baseband signal. MOS transistors generate large low frequency noise, of which the power density is inversely proportional to the frequency. Due to the lack of an IF amplifier, the downconverted signal is not strong enough to handle the flicker noise inside the baseband.

An *RC* highpass filter [7] or a servo feedback loop [8] can be applied after the downconversion mixer to attenuate the DC offset and the flicker noise. However, the highpass filter also works on the baseband signal and removes some useful signal power. A typical power spectrum of a 10 MHz raised-cosine filtered QPSK signal is shown in Figure 2.10. As we can see, the low frequency region contains a significant amount of the signal power, therefore the cut-off frequency of the highpass filter must be chosen carefully. A SIMULINK receiver model was setup to estimate the effect of the highpass filter on this QPSK signal. As illustrated in Figure 2.11, the 10 kHz and 500 kHz highpass filters reduce the SNR/bit

by about 0.5 dB and 3.5 dB respectively, thus the lower passband frequency the less effect of the SNR of the receiver.

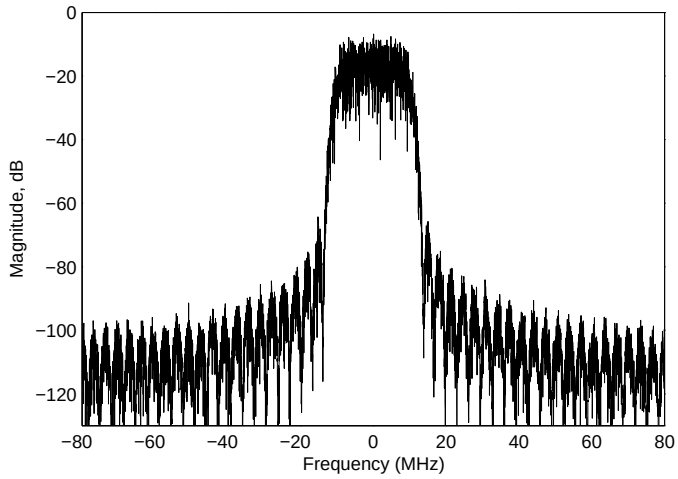

Figure 2.10. Spectrum of a raised-cosine filtered 10 MHz QPSK signal.

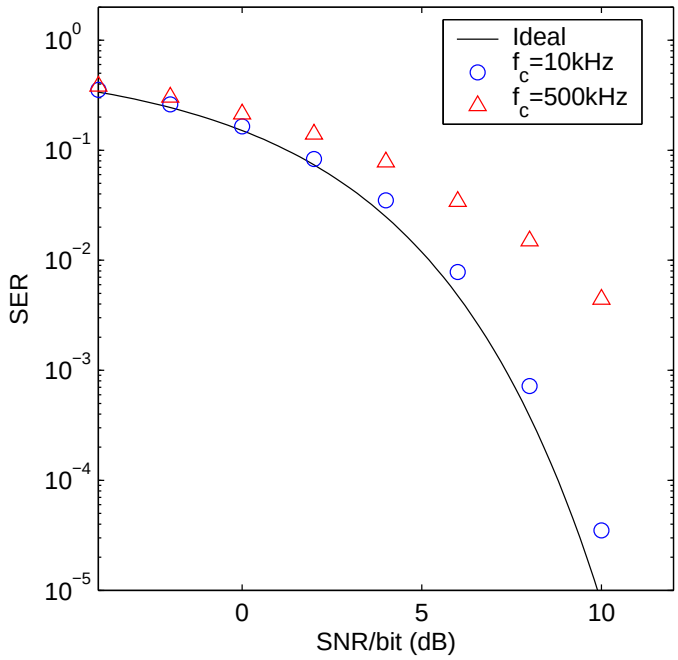

Figure 2.11. SERs of a received 10 MHz QPSK signal with a 10 kHz and a 500 kHz highpass filtering.

In addition to the DC offset, filtration of the flicker noise also needs particular attention. In order to numerically analysis the effect of flicker noise, the mean square inband noise power should be calculated. The receiver noise characteristics and the highpass filter frequency response are illustrated in Figure 2.12, where$f_{1/f}$ is the flicker noise corner

frequency, at which the flicker noise power is equal to that of the thermal noise; f_c is the cut-off frequency of the highpass filter and f_{BW} is the signal bandwidth. The total noise power inside the baseband is given by [9]

$$\begin{aligned} \overline{v_n^2} &= \overline{v_{1/f}^2} + \overline{v_{thm}^2} \\ &= \int_{f_c}^{f_{1/f}} \frac{K}{f} df + \int_{f_{1/f}}^{f_{BW}} S_{thm} df \\ &= S_{thm} \left[f_{BW} + f_{1/f} \ln\left(\frac{f_{1/f}}{f_c}\right) - f_{1/f} \right], \end{aligned} \tag{2.8}$$

where S_{thm} is the thermal noise spectrum density and $K = f_{1/f} S_{thm}$ is the flicker noise coefficient. Assuming $f_{1/f} = 300$ kHz and $f_c = 10$ kHz, for 1 MHz bandwidth, the total noise power $\overline{v_n^2} = 1.72(\text{MHz}) \times S_{thm}$. However, if the flicker noise is not included, the total noise power would be $1(\text{MHz}) \times S_{thm}$, which is 2.36 dB lower. The extra flicker noise power reduces the SNR by 2.4 dB. This value could be larger when the signal bandwidth is less than 1 MHz, as it is the case with GSM. Such a large SNR degradation prevents the implementation of direct downconversion receivers for narrow bandwidth applications.

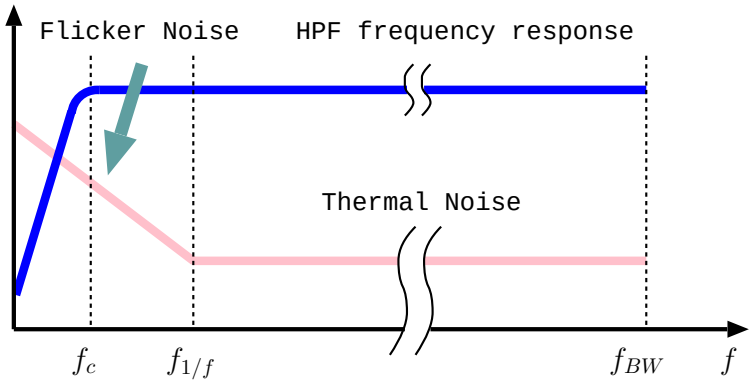

Figure 2.12. Receiver baseband noise spectrum and the highpass filter frequency response.

On the other hand, for large bandwidth applications, assuming $f_{BW} = 10$ MHz and following the same calculations described before, the total inband noise power only increases by 0.3 dB and reduces the SNR by about the same value. This value could even be smaller when modern SiGe BiCMOS technologies are utilised because the flicker noise introduced by bipolar transistors is be much less than that by MOS transistors.

This simple calculation gives an intuitive understanding: for the same flicker noise intensity in a wireless receiver, the larger signal bandwidth, the less performance degradation. Today's new wireless specifications, such as WCDMA, IEEE802.11a/b/g etc, all

occupy multi-megahertz bandwidth. This perhaps is the major reason that both academic and the industry researches focus on the development of direct downconversion receivers.

In a direct downconversion receiver, besides the low frequency non-idealities, the linearity of the baseband components are critical. After downconversion, there are still strong interferers in the vicinity of the baseband signal due to the lack of the IF bandpass filter. The third-order distortion of the interferers maybe located inside the baseband and corrupts the baseband signal, challenging the baseband analog circuit linearity.

In order to alleviate this challenge, the strong interferers after downconversion should be attenuated before any further amplification. Capacitive loads of the downconversion mixer can be employed to create a real pole at the band edge acting as a lowpass filter [8]. A highly linear Sallen-Key lowpass filter can be applied after the mixer to further suppress adjacent interferers [9].

In addition to the third-order distortion, the second-order distortion of the RF interferers generates a low frequency beat. A fraction of this low frequency beat may feedthrough the mixer due to the mismatch of the mixer differential paths. If the frequencies of the two strong interferers are close enough, this second-order distortion beat maybe located inside the baseband and corrupts the baseband signal.

The second-order distortion before mixer is introduced by the LNA only. Differential LNA circuitry with proper layout can largely suppress the second-order distortion. Moreover, the capacitive coupling between the LNA and the mixer also attenuates the second-order distortion beat due to the large impedance of a capacitor at low frequencies.

The design concerns discussed in this section strongly affect the implementation of direct downconversion receivers in the past. However, with the progress in the digital communication and RF integrated circuit technologies, these shortcomings can be solved or minimised to an acceptable level.

2.5 Summary

Receiver architectures including the heterodyne, image-rejection/low-IF and the homodyne are discussed in this chapter.

In heterodyne receivers, the gain stages and the bandpass filters at the RF and IF provide good sensitivity and selectivity. However the trade-off between image-rejection and channel-selection is a principle problem. The external IF filter and two downconversion stages increase the receiver complexity, power consumption, cost and reduce the system integration. The heterodyne architecture is a good (perhaps the only) candidate for narrow band (usually less then 1 MHz bandwidth) wireless receivers.

A low-IF receiver downconverts the RF to a very low IF to avoid the DC offset and the flicker noise. The image problem is alleviated by utilising image-rejection mixers. Because of the inevitable mismatch in the circuit realisation, an image-rejection mixer can only achieve limited IRR. Therefore, basically low-IF receivers are not suitable for most wireless systems due to the possible strong images. However, for some particular applications, such as a GPS C/A band receiver, there are no strong images presented. In such a cases, the low-IF architecture is a good choice to achieve a monolithic and low cost receiver.

In direct downconversion receivers, the image is just the RF signal itself, eliminating the image problem. The DC offset and the flicker noise are two major design issues that limited the implementation in the past. However, with today's large bandwidth communications, the non-idealities around DC cause negligible SNR loss. Linearity issues also can be minimised by proper layout and baseband circuitry design. With high integration, low power, low cost and moderate performance, direct downconversion receivers have become an active research and engineering topic.

In the next chapter, the specification of the IEEE802.11a standard for WLAN is introduced. The advantages of the direct downconversion architecture for IEEE802.11a receivers are further discussed. Also system level receiver performance limitations due to the direct downconversion non-idealities are analysed.

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Chapter 3

IEEE802.11a Receiver System Level Analysis

3.1 Introduction

The general analysis presented in Chapter 2 shows that for broadband wireless applications, direct downconversion receiver impairments related to zero IF can be minimised to an acceptable level. An IEEE802.11a transmission channel occupies 20 MHz at the passband that satisfies the large bandwidth requirement. In addition, there is a so-called zero-padding technique in the IEEE802.11a OFDM modulation, which further suppresses the effect of low frequency non-idealities and makes the direct downconversion architecture more attractive.

In this chapter, the receiver aspects for the IEEE802.11a standard are discussed. The IEEE802.11a physical layer themes are first introduced. Next, the fundamentals of pulse shaping for zero ISI are discussed. Finally, the receiver limitations due to the thermal noise, flicker noise, phase noise, and the I/Q gain and phase mismatches are analysed.

3.2 IEEE802.11a Physical Link

The IEEE802.11a standard specifies operation in the U-NII band at 5 GHz. Unlike IEEE802.11b that uses DSSS, IEEE802.11a employs OFDM modulation to achieve better

indoor performance. As illustrated in Figure 3.1, there are two contiguous band from 5.15 GHz to 5.35 GHz with the maximum transmission power of 40 mW and 200 mW respectively, and a separate band from 5.725 GHz to 5.825 GHz with the maximum power of 800 mW. Each IEEE802.11a RF band accommodates 4 carriers spaced by 20 MHz. The outermost carriers in the contiguous lower and middle bands shall be at a distance of 30 MHz from the band edge, and 20 MHz for the upper band. Each carrier is subdivided into 52 subcarriers, among which, 48 are for data transmission and the remaining 4 for error correction. The subcarrier frequencies are chosen to be orthogonal, therefore unlike FDM, overlapped spectrum extensions between subcarriers are allowed to improve the spectrum efficiency.

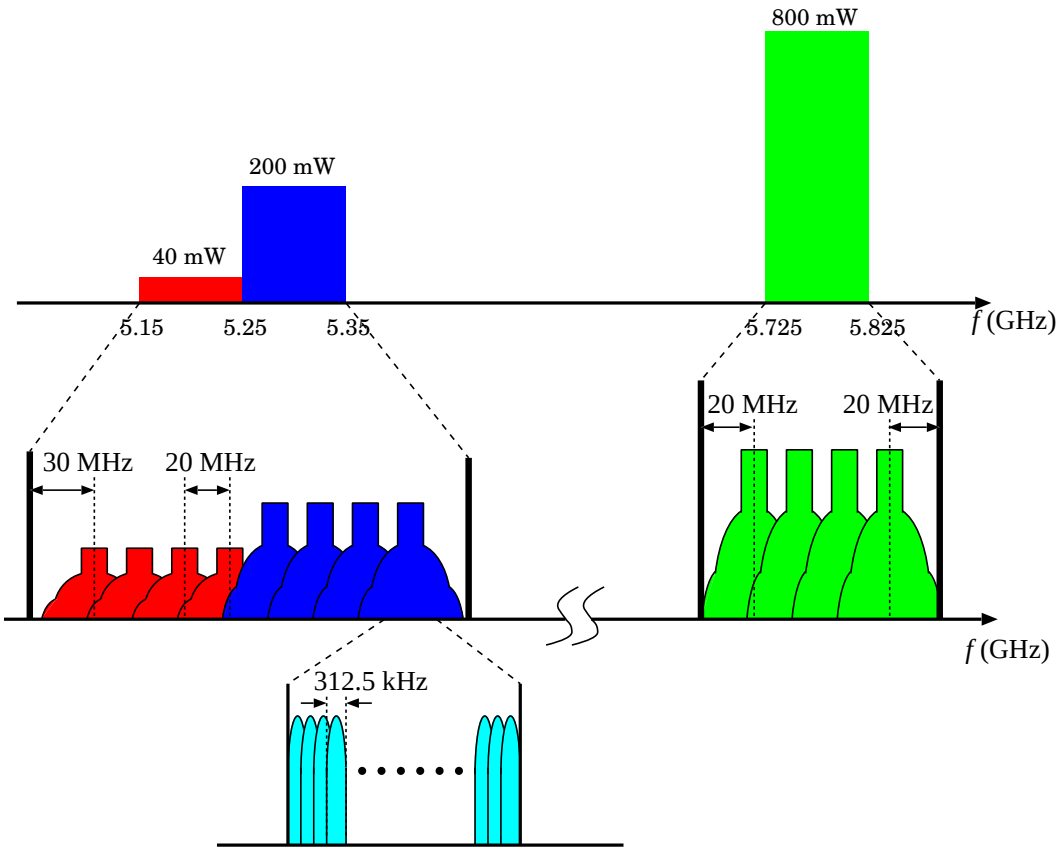


Figure 3.1. IEEE802.11a OFDM PHY frequency channel plan.

The 48 data subcarriers can be either BPSK, QPSK, 16-QAM, or 64-QAM modulated signals, depending on the channel quality. At the lowest data rate, BPSK modulates 187.5 Kbps of data per subcarrier, resulting in 9 Mbps data rate. Using QPSK modulation, it doubles to 18 Mbps, and to 36 Mbps when using 16-QAM. The highest data rate of 54

Mbps can be achieved when using 64-QAM that enables video communications over the IEEE802.11a WLAN. The 4 pilot subcarriers for error correction utilise slow but reliable BPSK modulation.

The orthogonal subcarrier frequencies can be generated in the digital frequency domain using the IFFT algorithm. As demonstrated in Figure 3.2, a 64-channel hardware IFFT is utilised to transform the digital constellation sequence into a time domain complex signal. This complex signal experiences pulse shaping and I, Q modulation, and then is upconverted to the RF for transmission. At the receiver end, the radio signal passes through the downconversion, demodulation processes, and eventually is returned to the constellations by an FFT machine. The IFFT output sequence of an OFDM symbol can be expressed as

$$x_n = \frac{1}{N}\sum_{i=0}^{N-1} X_i e^{2\pi jni/N}, \qquad (n = 0, 1, 2, \cdots, N-1) \tag{3.1}$$

where, N is the subcarrier number and X_i is a symbol. At the receiver end, the FFT output sequence of the OFDM symbol is then given by

$$\begin{aligned} Y_k &= \sum_{n=0}^{N-1} x_n e^{-2\pi jnk/N} \\ &= \sum_{n=0}^{N-1} \frac{1}{N} \sum_{i=0}^{N-1} X_i e^{2\pi jn(i-k)/N} \\ &= \begin{cases} X_k, & i = k \\ 0. & i \neq k \end{cases} \qquad (i = 0, 1, 2..., N-1) \end{aligned} \tag{3.2}$$

The IFFT and the FFT function blocks contain 64-channels, however the total subcarrier number is only 52, therefore 12 zeroed channels are added as dummies. This process is named zero-padding. 10 dummy subcarriers are put at the band edge to relax the channel-selection filtering and the remaining 2 are put at DC to alleviate the low frequency impairments including the DC offset and the flicker noise. Because of the zero-padded first channel, the direct downconversion architecture is more suitable for the IEEE802.11a OFDM standard than others that use DSSS modulation, such as IEEE802.11b. A simple first-order RC highpass filter can be employed to suppress the DC offset and having negligible effect on the data if the filter stopband is much less than 300 kHz. An IEEE802.11a PHY SIMULINK model [10] is utilised to simulated the SER.

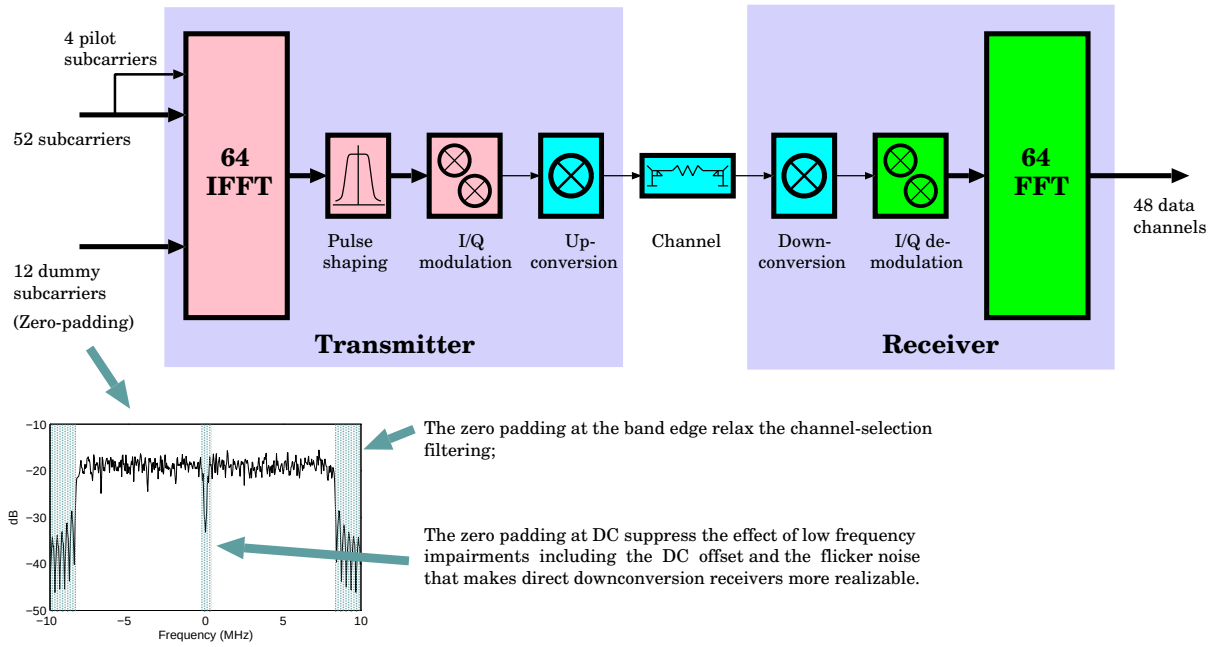


Figure 3.2. IEEE802.11a PHY link. The zero-padding technique makes the direct downconversion architecture more feasible.

As demonstrated in Figure 3.3, the SER results with and without a 10 kHz highpass filter are about the same that confirms the analysis.

The required receiver noise figure can be calculated from the IEEE802.11a standard and the receiver sensitivity expression as [7]

$$S(\text{dB}) = 174(\text{dBm}) - NF(\text{dB}) - 10\log(BW) - SNR(\text{dB}), \tag{3.3}$$

where NF is the noise figure, $BW = 16.25$ MHz is the channel bandwidth at the passband and $SNR(dB)$ is the signal-to-noise ratio. The noise figure can be calculated when all the other variables are determined. As an example, for the highest data rate using 64-QAM, S requires -66 dBm. Substituting S and BW into Eq. 3.3 yields the combined NF and SNR as

$$\begin{aligned} NF + SNR &= 174(\text{dBm}) - |S(\text{dBm})| - 10\log(BW) \\ &= 36 \text{ dB}. \end{aligned} \tag{3.4}$$

Assuming a 28 dB SNR when considering the 64-QAM modulation, the maximum receiver noise figure should not exceed 8 dB.

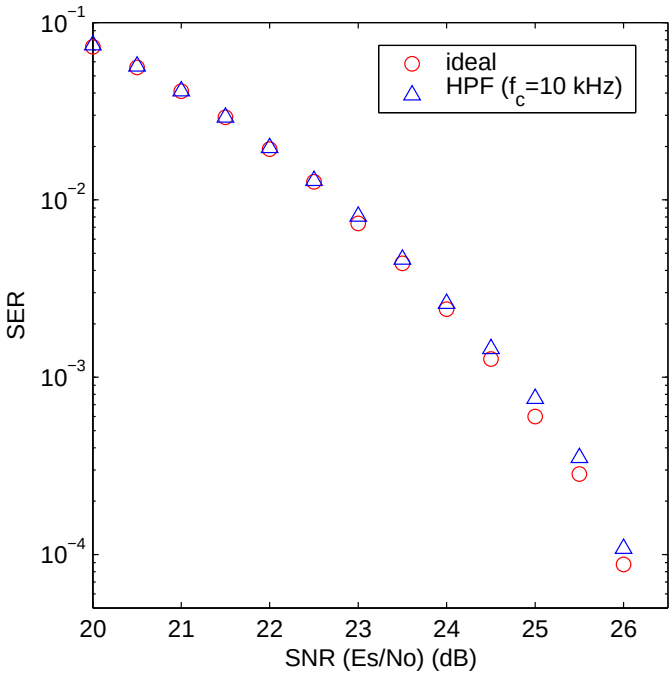


Figure 3.3. SERs of the 64-QAM modulated 802.11a PHY link with zero-padding technique.

The IEEE802.11a specification requires the maximum input RF signal power of -30 dBm. This indicates that the receiver input referred 1 dB gain compression point should be greater than -30 dBm.

3.3 Pulse Shaping and Raised Cosine-Rolloff Filter

In a digital modulation system, the baseband signal is in digital format and presented as a rectangular pulse sequence to modulate the RF carrier. The sharp rectangular pulse edge contains rich frequency components. This can be explained as that the Fourier transform of a square window is a sinc function in the frequency domain. As illustrated in Figure 3.4, the first sidelobe of a QPSK signal spectrum is only 13 dB lower than the the mainlobe. This is an unacceptable spectrum efficiency because the adjacent channel must be separated sufficiently far to avoid the interference. Therefore the rectangular pulses must be shaped to attenuate the sidelobes before modulating the RF carrier. This process is referred to as pulse shaping and is achieved using a lowpass filter. However, the lowpass filtration of a square pulse train introduces ISI problem.

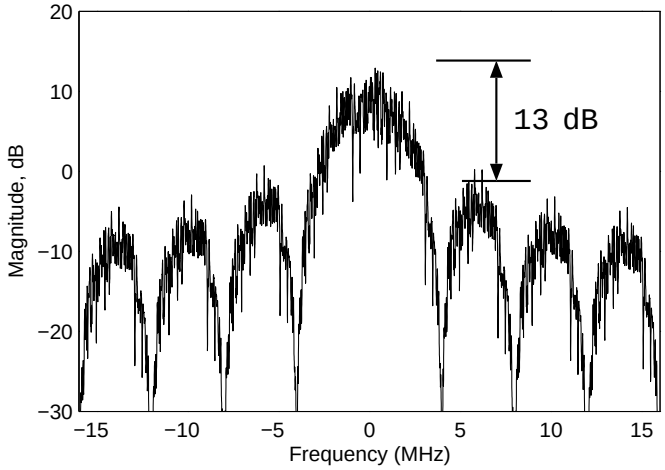


Figure 3.4. Spectrum of a QPSK signal at baseband without pulse shaping.

Figure 3.5 shows a digital sequence passing through a lowpass filter. The filtered pulses tend to get elongated tails and smear into the nearby pulses. The circled areas show strong interference by the energy tails. This kind of interference between digital symbols, discovered by Morse, is defined as the ISI. Nyquist first studied this issue and developed three possible solutions [11] to control the ISI, among which raised cosine-rolloff filters are widely used in today's digital communication systems.

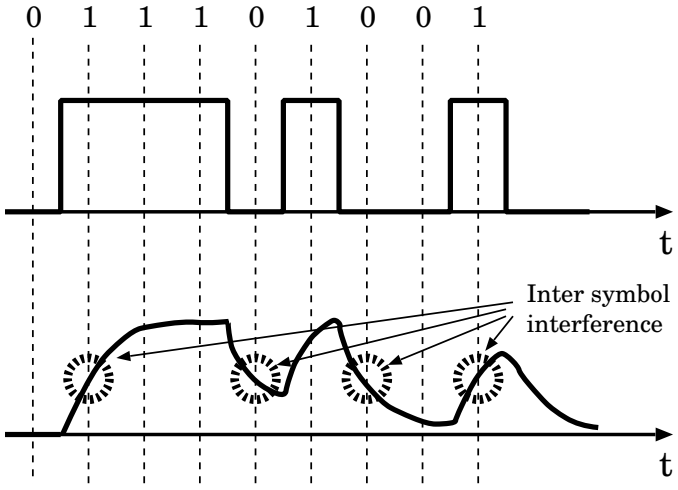


Figure 3.5. Inter symbol interference.

In a discrete system, the sampled signal can be represented by a pulse train as

$$x_s = \sum_n x(nT_s)\delta(t - nT_s) \tag{3.5}$$

where, T_s is the sampling period and δ is the Delta function. Assuming the impulse response of a lowpass filter is $h(t)$, then the output signal is given by

$$\begin{aligned} y_s(t) &= \int_{-\infty}^{+\infty} \left[\sum_n x(nT_s)\delta(t-nT_s) \right] h(t-\tau)d\tau \\ &= \sum_n x(nT_s)h(t-nT_s). \end{aligned} \tag{3.6}$$

In a discrete lowpass filter system, in order to have zero ISI, the output should be equal to the input at the sampling points, yielding

$$h(kT_s - nT_s) = \begin{cases} 1, & k = n \\ 0. & k \neq n \end{cases} \tag{3.7}$$

Eq. 3.7 is Nyquist's first criterion for zero ISI. The sinc function is a good candidate for the lowpass filter, because by controlling its frequency, Nyquist's first zero ISI criterion can be satisfied. Substituting a sinc function into Eq. 3.6, the sampled output y_s becomes

$$\begin{aligned} y_s(t) &= \sum_n x(nT_s)\frac{\omega T_s}{\pi}\frac{\sin[\omega(t-nT_s)]}{\omega(t-nT_s)}\Bigg|_{t=kT_s,\ \omega=2\pi N/T_s} \\ &= \sum_n x(nT_s)\delta(kT_s - nT_s), \end{aligned} \tag{3.8}$$

where $\omega = 2\pi N/T_s$ is the frequency of the sinc function in radians and N is an integer. From Eq. 3.5 and Eq. 3.8, we can see that the data before and after filtering are the same at the sampling points, resulting in zero ISI. Figure 3.6 shows the sampled data and the zero ISI filtered output with $\omega = 2\pi/T_s$ (N=1).

However, sinc function impulse response is not causal (the frequency response is a square window) hence not achievable. In addition, sinc function decays too slow, thus inaccurate samples (for example due to the clock jitter) cause ISI. The raised cosine-rolloff filter has smoother frequency response and faster decay. In the frequency domain, the transfer function of a raised cosine-rolloff filter is defined as

$$H(f) = \begin{cases} 1, & 0 < |f| < \frac{1-\alpha}{2T_s} \\ \frac{1}{2}\left[1 + \cos\frac{\pi T_s}{\alpha}\left(|f| - \frac{1-\alpha}{2T_s}\right)\right], & \frac{1-\alpha}{2T_s} < |f| < \frac{1+\alpha}{2T_s} \\ 0. & |f| > \frac{1+\alpha}{2T_s} \end{cases} \tag{3.9}$$

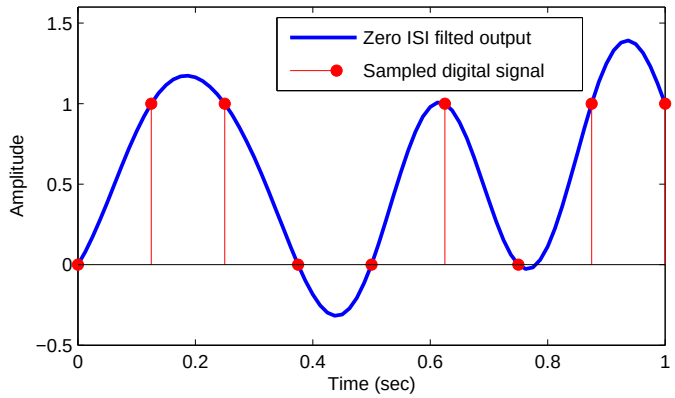


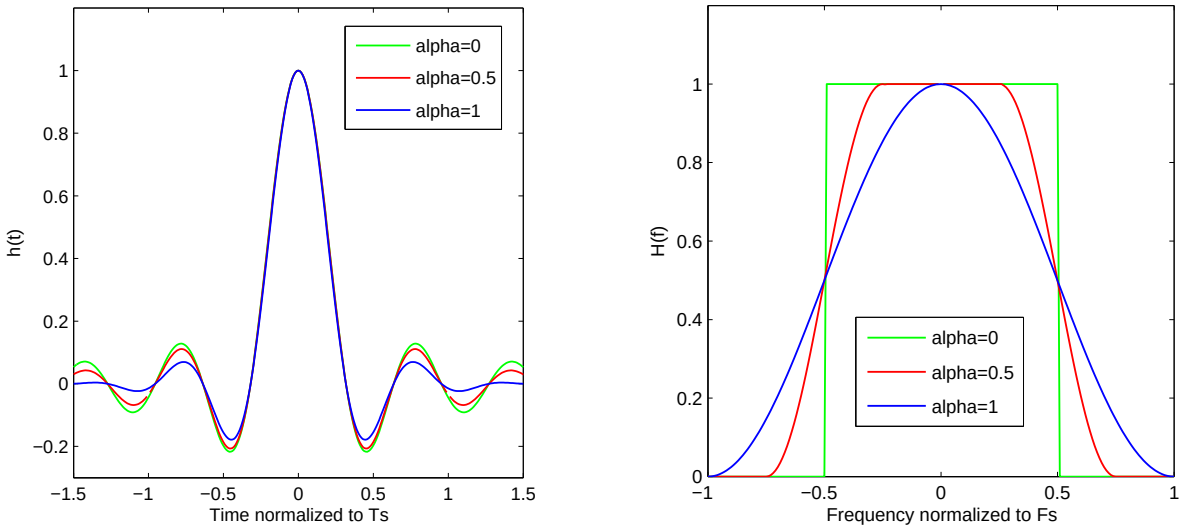
Figure 3.6. Discrete signal and zero ISI filtered output.

where $0 < \alpha < 1$ is the rolloff factor and T_s is the sampling frequency. In the time domain, the impulse response is given by

$$h(t) = \frac{\sin(\pi t/T_s)}{\pi t/T_s} \frac{\cos(\pi \alpha t/T_s)}{1 - 4\alpha^2 t^2/T_s^2}. \tag{3.10}$$

Figure 3.7 shows the plots of the frequency and impulse responses of a raised cosine-rolloff filter with different values of α. The first term of Eq. 3.10 is a sinc function, so that it satisfies Nyquist's first criterion for zero ISI. When α is equal to zero, $h(t)$ degrades to a sinc function. From the frequency responses shown in Figure 3.7(b), we can find that the excess bandwidth (with respect to the square window) is increasing by a factor of $1 + \alpha$ as long as the rolloff factor α is increasing. For example, assuming the symbol rate is 8.45 Msps, when a raised cosine-rolloff filter is applied for the pulse shaping, the minimum bandwidth required at the passband is $2 \times 8.45 = 16.9$ MHz for $\alpha = 0$; $2 \times 8.45 \times (1 + 0.3) = 22$ MHz for $\alpha = 0.3$, and $2 \times 8.45 \times (1 + 0.5) = 25.35$ MHz for $\alpha = 0.5$. Therefore, a smaller α brings better spectrum efficiency, but harder to achieve due to its sharper cut-off frequency response.

An ideal raised cosine-rolloff filter is also non-causal, because its impulse response extends to $\pm\infty$. However, since the impulse response decays rapidly, especially for larger α, it is reasonable to only select a segment of the impulse response for the pulse-shaping. As depicted in Figure 3.8, the selected raised cosine-rolloff impulse response should shift right along the time axis to make the initial response at the time origin. The right shift of the impulse response introduces group delay, defined as the time of the mainlobe peak. Group delay must be compensated for when doing SER simulations by comparing the transmitted and the received symbols.



(a) (b)

Figure 3.7. (a) Impulse and (b) frequency responses of a raised cosine-rolloff filter with different α values.

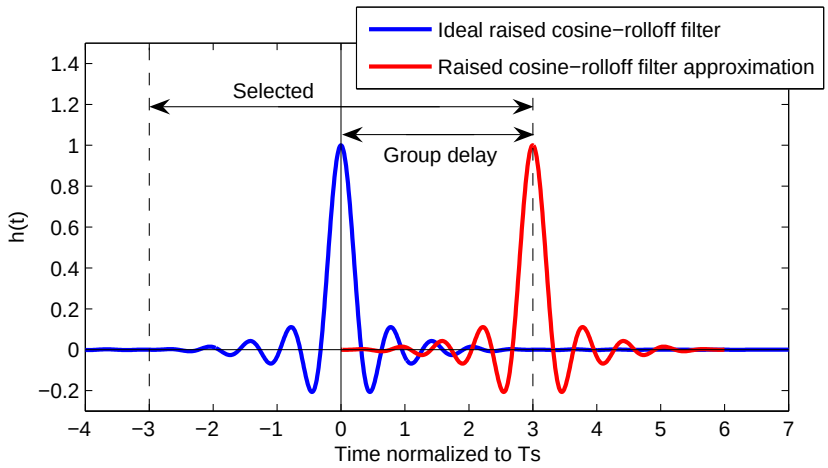
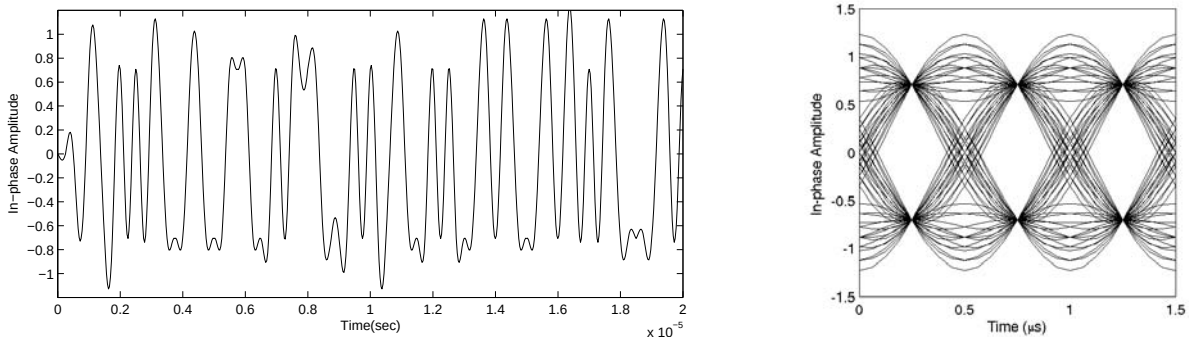


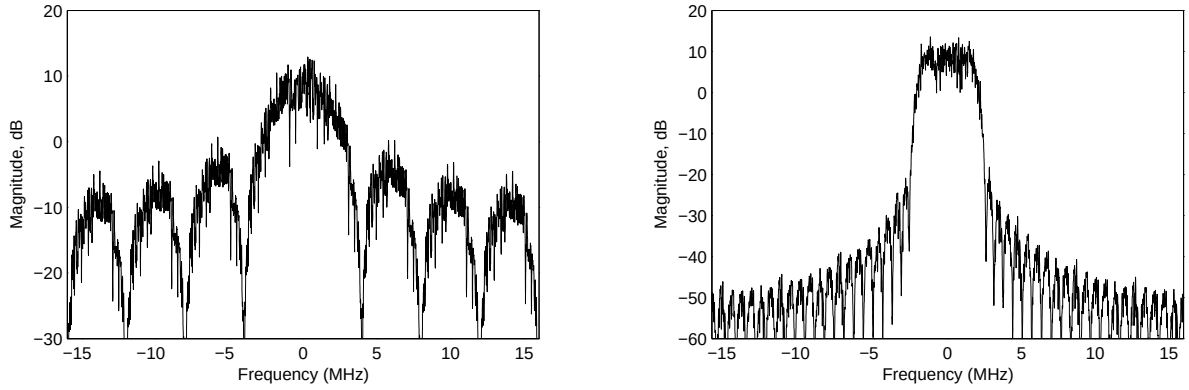
Figure 3.8. Raised cosine-rolloff filter approximation.

Figure 3.9 shows a raised cosine-rolloff filtered QPSK inphase channel in the time domain and its eye-diagram with a rolloff factor of 0.3. The spectrum of an unshaped and shaped QPSK signal at the baseband are presented in Figure 3.10. The sidelobes are greatly attenuated by the pulse shaping filtration, resulting in better spectrum efficiency.



(a) (b)

Figure 3.9. Raised cosine-rolloff filtered QPSK signal. (a) Time domain waveform; (b) eye-diagram.



(a) (b)

Figure 3.10. Spectrum of a QPSK signal at the baseband. (a) Without pulse shaping; (b) raised cosine-rolloff filtered (α=0.3).

3.4 Thermal Noise

Thermal noise is a fundamental noise source in all electronic devices. The understanding of the thermal noise can be backtracked to the 19th century. Because of the successful development of high gain amplifiers, engineers believed that they could amplify any received signals in a communication system regardless their weakness. Soon they found that when the signal power was lower than a certain level, the amplified output was no longer the signal but a white noise. It seemed that there was a white noise floor, which limited the device sensitivity; hence thermal noise was discovered.

Thermal noise is generated by the random motion of electrons in any electronic devices. In a resistor, the mean square thermal noise voltage can be presented as

$$\overline{V^2} = 4kTR\Delta f, \tag{3.11}$$

where k is the Boltzmann constant, T is the absolute temperature, R is the resistance and Δf is the measurement bandwidth. Thermal noise theoretically has unlimited power, since its PSD extends from $-\infty$ to $+\infty$ along the frequency axis. In reality, the noise power inside a measurement bandwidth Δf is used and has a unit of V^2/Hz.

In a MOS transistor, the thermal noise mean square current can be derived by the equivalent channel resistance as

$$\overline{i^2} = 4kT\gamma g_{d0}\Delta f, \tag{3.12}$$

where g_{d0} is the transistor conductance when the drain to source voltage V_{ds} is 0 V, γ is a process related constant. For long channel processes, γ is equal to 2/3 when the MOSFET is biased in the saturation region [12]. For submicron and deep submicron process, γ exhibits a much larger value, which can be 2∼3 in saturation, or even higher [13].

The thermal noise amplitude has a Gaussian probability distribution. For numerical analysis, the signal is therefore assumed to be corrupted by the addition of the white Gaussian noise. The SER probability of an M-ary QAM signal corrupted by the AWGN is given by [14]

$$P_M = 1 - \left[1 - 2\left(1 - \frac{1}{\sqrt{M}}\right) Q\left(\sqrt{\frac{3k}{(M-1)}\frac{E_b}{N_0}}\right)\right]^2, \tag{3.13}$$

where E_b is the energy in a bit, $N_0/2$ is the white Gaussian noise spectrum density, E_b/N_0 represents the average SNR per bit, $k = \log_2 M$, and Q is the Q-function defined as

$$\begin{aligned} Q(x) &= \frac{1}{\sqrt{2\pi}}\int_x^\infty e^{-t^2/2}dt, \qquad x \geq 0 \\ &= \frac{1}{2}\mathrm{erfc}\left(\frac{x}{\sqrt{2}}\right). \end{aligned} \tag{3.14}$$

The IEEE802.11a SIMULINK model for the SER simulation is illustrated in Figure 3.11. Either B/QPSK or QAM modulations can be utilised for the 52 data channels (including 4 pilot channels). Extra 12 dummy channels are added for the zero-padding,

according to the specification. An AWGN blockset is employed to represent the thermal noise. The calculated P_M results using Eq. 3.13 and the simulated SERs are shown in Figure 3.12. To achieve 10% SER for QPSK, 16-QAM and 64-QAM modulations, the required SNR/bit are 1.25 dB, 6.18 dB and 10.97 dB, respectively.

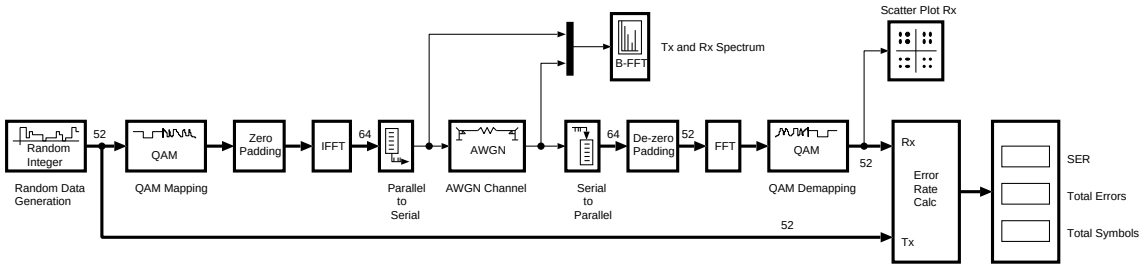


Figure 3.11. IEEE802.11a PHY link SIMULINK model for SER simulations.

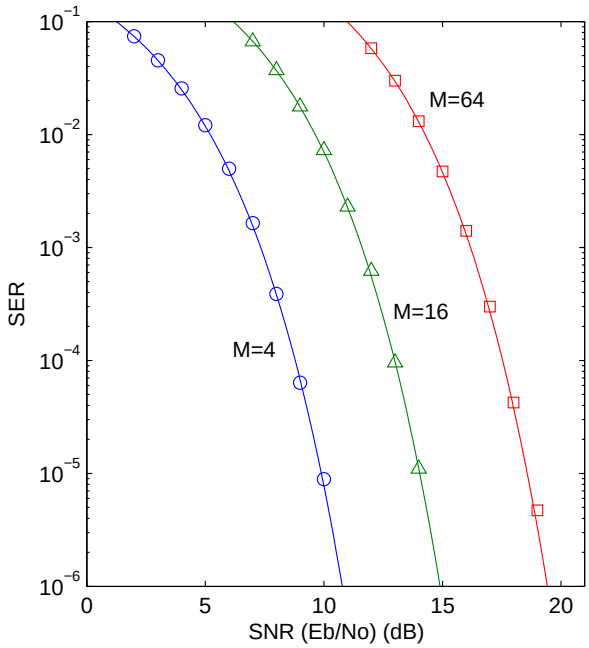


Figure 3.12. Simulated (symbols) and calculated (lines) SERs of the IEEE802.11a PHY link corrupted by the thermal noise.

3.5 Flicker Noise

Another critical noise source in electronic devices is flicker noise, also named as $1/f$ noise or pink noise. Early work on the flicker noise in MOSFETs was started in the middle

of 1960s, when MOS processes were improved to allow the integration of analog circuits. Till now, universal agreement on the flicker noise mechanism is still hard to identify [13]. However in MOSFETs, the major mechanism of the flicker noise is the non-ideality of the Si/SiO2 interface characterisation. The gate interface defects induced flicker noise in MOSFETs is much larger than that in bipolar transistors, which is due to the base current flowing through forward biased PN junctions [13]. Therefore it is significantly important to analyse the flicker noise when using MOS processes, especially for direct downconversion architectures, as discussed in chapter 2.

The flicker noise mean square current in the measurement bandwidth Δf is inversely proportional to the frequency. In a MOSFET it is given by

$$\overline{i_n^2} = \frac{K}{f}\frac{g_m^2}{AC_{ox}^2}\Delta f, \tag{3.15}$$

where $A = WL$ is the channel area, C_{ox} is the gate oxide capacitance, g_m is the transconductance, and K is a process related constant with a reasonable value between 10^{-19} to 10^{-25} V^2F [15]. By Thevenin Equivalent, the flicker noise also can be presented in the mean square voltage form as

$$\overline{v_n^2} = \frac{K}{f}\frac{1}{AC_{ox}}\Delta f. \tag{3.16}$$

The PSD of the flicker noise and the thermal noise is demonstrated in Figure 3.13. At low frequencies, the flicker noise power is significantly large. As the frequency increases, the flicker noise PSD drops linearly on a logarithmic plot until merging into the thermal noise floor. The frequency, where the PSD of the flicker noise equals to that of the thermal noise, is defined as the flicker noise corner frequency, which has a typical value of several hundred kilohertz in a MOSFET.

For the simulation purpose, a flicker noise source can be obtained by passing a white noise through a lowpass filter, which has a magnitude response given by [16]

$$|H(f)| = \frac{1}{\sqrt{f}}. \tag{3.17}$$

In SIMULINK, to achieve a realisable lowpass transfer function, the ideal $1/\sqrt{f}$ filter can be approximated by a discrete transfer function in the z-domain as

$$H(z) = \frac{0.049922 - 0.0959935z^{-1} + 0.0506127z^{-2} - 0.0044088z^{-3}}{1 - 2.494956z^{-1} + 2.0172659z^{-2} - 0.5221894z^{-3}}. \tag{3.18}$$

The frequency response of Eq. 3.18 is plotted in Figure 3.14. By feeding white noise into this filter, pink noise can be obtained. The original white noise and the output flicker

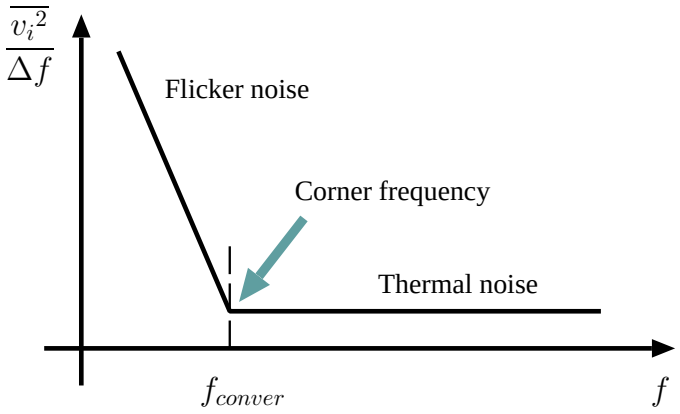


Figure 3.13. PSDs of the flicker noise and the thermal noise.

noise in the time domain are shown in Figure 3.15. The flicker noise PSD can be evaluated by spectrum analysis.

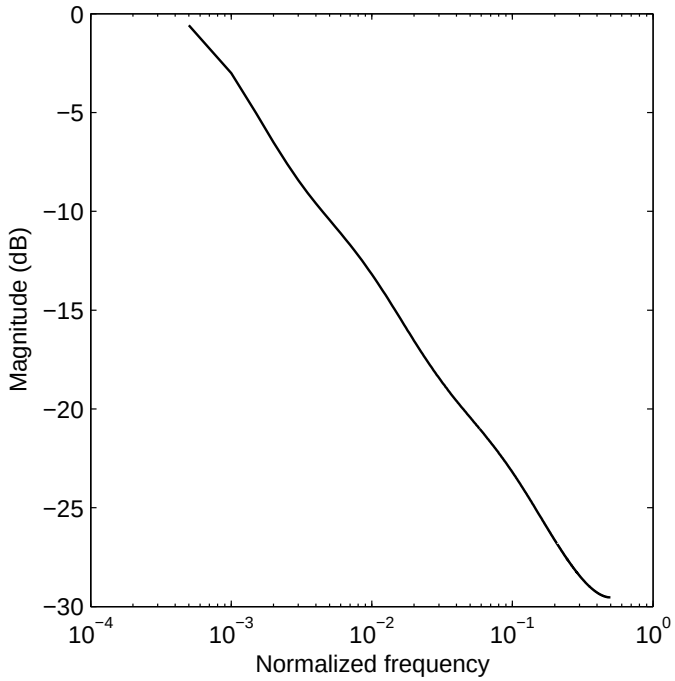


Figure 3.14. Frequency response of the discrete filter of Eq. 3.18.

The periodogram method, which takes a modulus-squared FFT of a finite discrete series, is often used for PSD estimations. However, the spectrum uncertainty problem is a main drawback of this method. This can be explained as that the PSD over a frequency bin of a continuous function is estimated by a single point periodogram centred at the

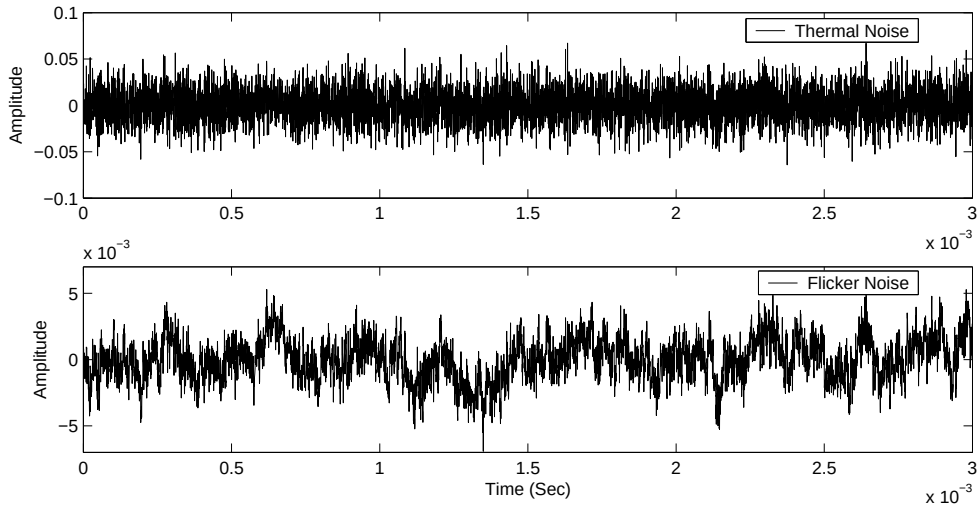


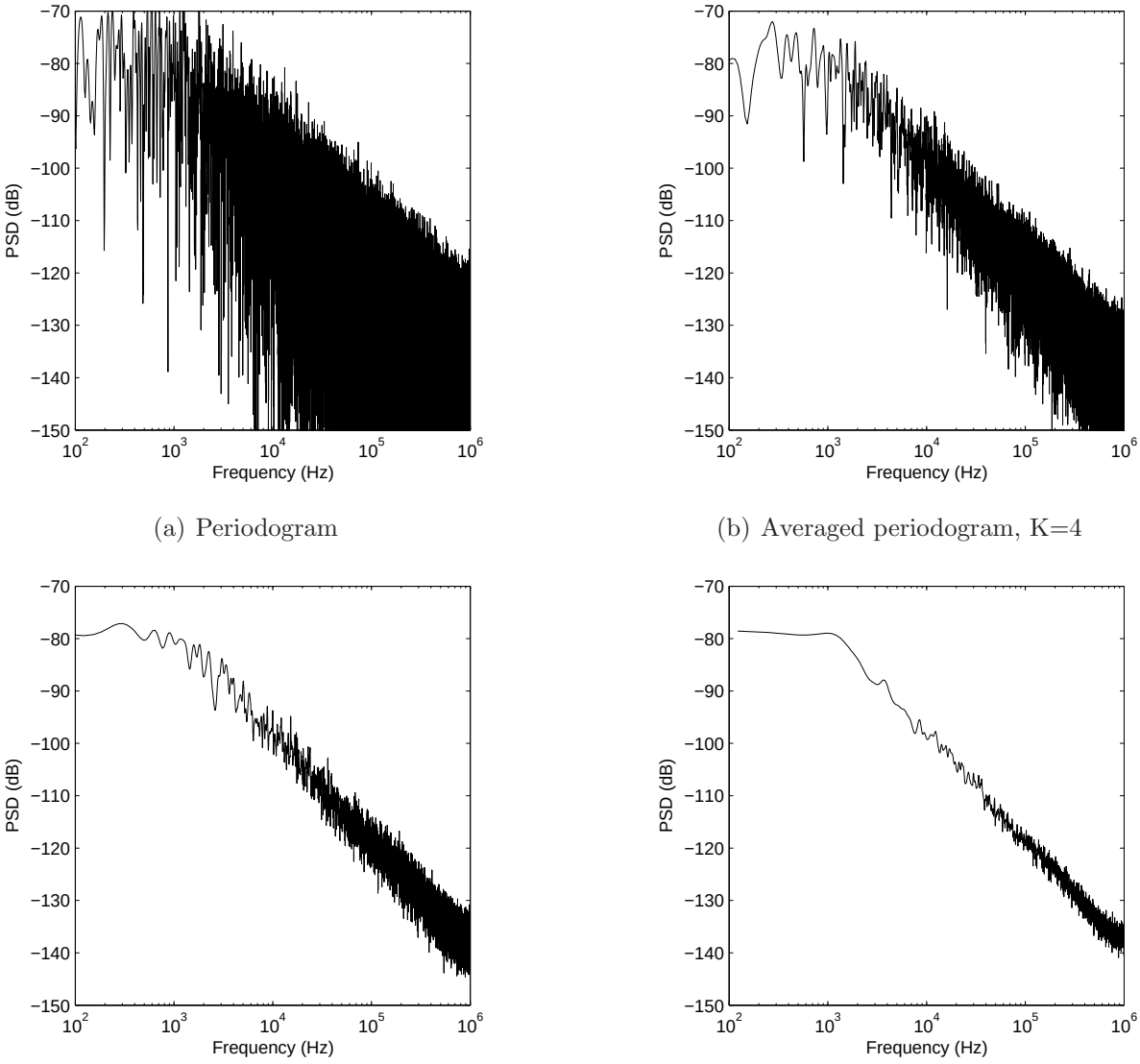
Figure 3.15. Thermal noise source and the output flicker noise.

frequency bin, resulting in 100 percent standard deviation [17]. Moreover, the standard deviation does not improve when increasing the sampled data sequence.

In order to reduce the variance of the estimates, the original data sequence can be split into K segments to apply periodogram estimations separately, then averaging the K periodogram estimations. This technique is called averaged periodogram, which reduces the variance by a factor K or standard deviation by a factor $\sqrt{K}$. The flicker noise PSDs using the averaged periodogram with different K values are illustrated in Figure 3.16. The averaged periodogram technique is also used for the Sigma-Delta modulator spectrum analysis in Chapters 5 and 6.

In an IEEE802.11a OFDM system, since the first 312.5 kHz subcarrier is zero-padded, the flicker noise effect is much reduced. To simulate the receiver SER corrupted by the flicker noise, the $1/f$ shaped noise source is added into the receiver SIMULINK model illustrated in Figure 3.11. The simulated SERs are shown in Figure 3.17. From the graphic, we can see that for the high order M-ary modulation, the SER is sensitive to the flicker noise out of the first dummy channel. Hence, the receiver noise figure needs to be carefully evaluated in the low frequency region.

In a direct downconversion receiver, the critical flicker noise is introduced by the mixer, the frontend to baseband interface circuitry, and the first baseband amplifier. The circuit level design concerns about the flicker noise are discussed in Chapter 4.



(a) Periodogram

(b) Averaged periodogram, K=4

(c) Averaged periodogram, K=16

(d) Averaged periodogram, K=64

Figure 3.16. Flicker noise PSD estimated by the averaged periodogram method.

3.6 Phase Noise

Phase noise is another important noise source introduced by local oscillators in wireless receivers. An ideal local oscillator generates a sinusoidal signal with a single beat spectrum located at f_{LO} in the frequency domain. However, in practise the LO spectrum appears a skirt-like leakage to the nearby frequency region centred at f_{LO}, as illustrated in Figure 3.18. The leaked LO signal downconverts and spreads the spectrum of both the desired signal and the interferers in the vicinity. Since the interferers maybe significantly

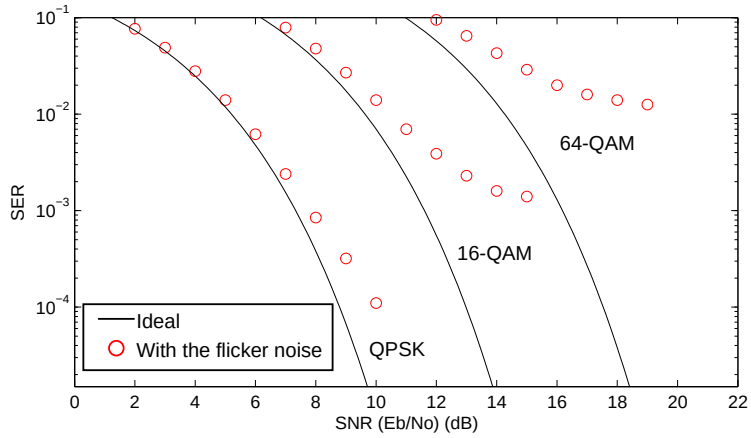


Figure 3.17. Simulated SERs of the IEEE802.11a PHY link corrupted by the flicker noise.

stronger than the desired signal, the spectrum leakage of the interferers is suspectable to corrupt the baseband signal, as depicted in Figure 3.19.

(a) (b)

Figure 3.18. LO spectrum. (a) Ideal; (b) with the phase noise.

In addition to spreading the interferer spectrum, the LO phase noise affects the baseband signal directly. The uncertain LO phase corrupts the information contained in the phase of the RF carrier. Figure 3.20 illustrates the typical constellation of a 64-QAM signal corrupted by the LO phase noise with 2 degrees error. In an IEEE802.11a receiver, the typical rotated constellations due to the phase noise cannot be seen, because the 64 parallel IFFT channels are interleaved and converted into a serial sequence before passing through the I, Q mixers.

The SIMULINK model shown in Figure 3.11 was used with the phase noise blockset added in the AWGN channel to simulate the SER corrupted by the phase noise. The simulation results are shown in Figure 3.21. The higher M-ary modulation requires tighter

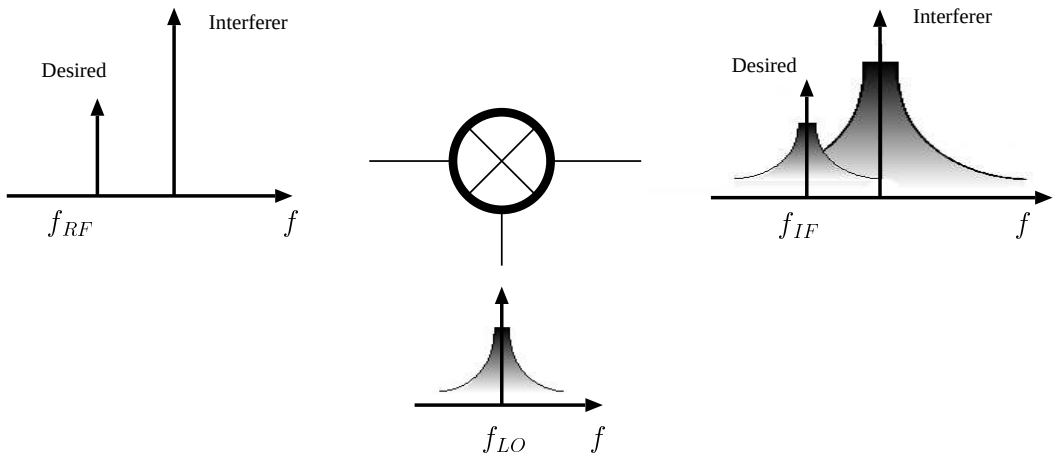


Figure 3.19. Reciprocal mixing.

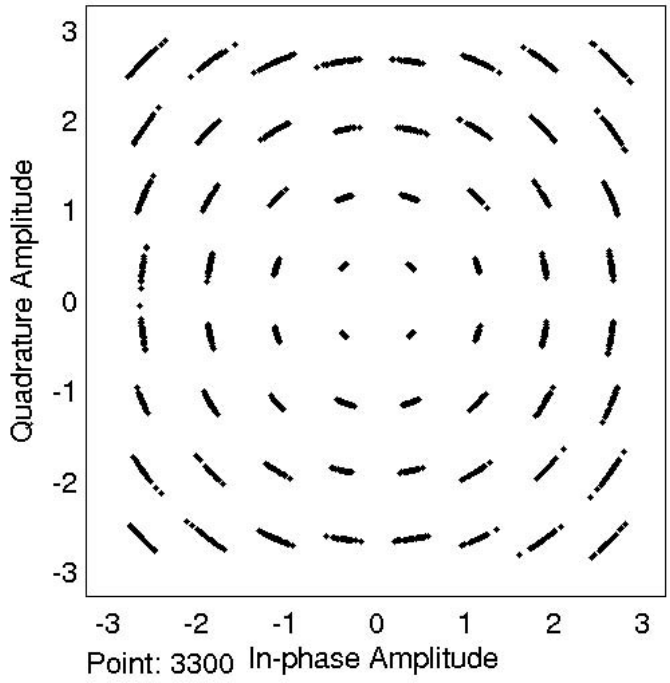


Figure 3.20. Constellation of a 64-QAM signal corrupted the phase noise with 2 degrees error.

phase noise criteria. To maintain a 0.1% SER, 8°, 4° and 2° phase errors introduce about 1 dB SNR/bit loss for QPSK, 16-QAM and 64-QAM modulations, respectively.

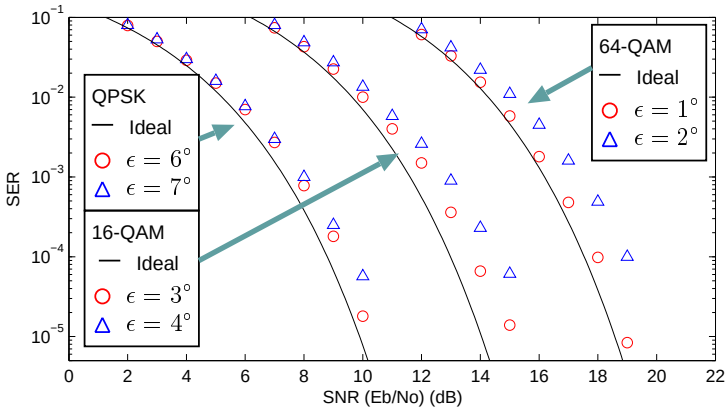


Figure 3.21. Simulated SER of the IEEE802.11a PHY link corrupted by the phase noise.

3.7 Quadrature Mismatch

In order to save the bandwidth, quadrature modulation is often used in today's communication systems, so that receivers must incorporate quadrature downconversion. In such quadrature receivers, mismatch problems appear in terms of gain and phase mismatches along the I and Q paths.

A quadrature downconversion stage is shown in Figure 3.22. The quadrature RF signal is frequency translated to baseband through the I and Q paths in parallel. The gains along the I, Q paths are assumed identical for the ideal model. However, in circuit realisations, gain imbalance between the two paths is inevitable. Assuming that the received RF signal is $I(t)\cos(\omega_{RF}t) + Q(t)\sin(\omega_{RF}t)$ and the I, Q gains are A and $A+\varepsilon$ respectively, where ε represent the gain error, the I, Q outputs are then given by

$$out_I = \frac{A}{2} I(t), \tag{3.19}$$

$$out_Q = \frac{A}{2}\left(1 + \frac{\varepsilon}{A}\right) Q(t). \tag{3.20}$$

The effect of the gain mismatch on a QPSK signal is illustrated in Figure 3.23. The hollow circles indicate the ideal QPSK constellation separated by D_0 between two antipodal symbols. The filled circles are the QPSK constellation with the Q path gain error ε. The distance between the antipodal symbols along the I and Q paths are D_0 and $D_0 + D_0\varepsilon/A$ respectively. As depicted in Figure 3.23, when the QPSK signal is corrupted by AWGN, the SER is determined by the Gaussian distributed noise amplitude and the signal energy, which is related to D_0. Along the I path, the BER is equal to the ideal

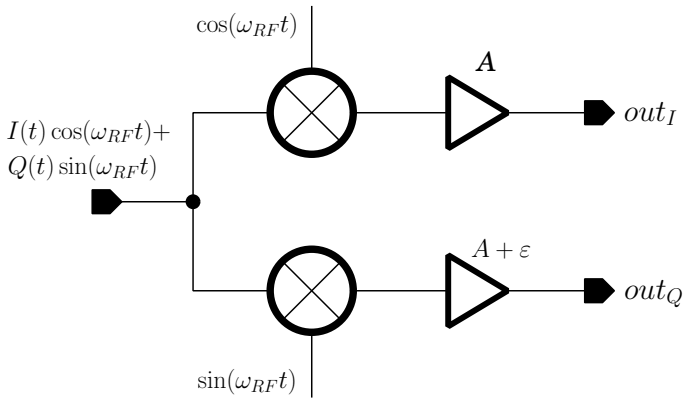


Figure 3.22. Downconversion with the I, Q gain mismatch.

case since the symbol distance is unchanged. For the Q path, when the gain error ε is positive, the symbols along Q path are more spread, thereby improves the BER with the penalty of more energy dissipation. When ε is negative, on the other hand, the symbols are closer, reducing the BER.

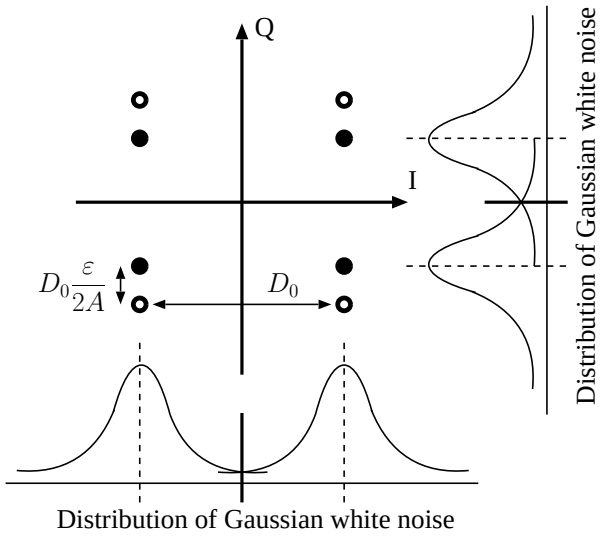


Figure 3.23. Effect of the I, Q gain mismatch on a QPSK signal.

For the IEEE802.11a OFDM modulation, the I and Q gain mismatch destroys the orthogonality between the subcarriers. So that Eq. 3.2 is no longer zero when $i \neq k$, allowing the symbol leakage from other subcarriers. The simulated SERs in the case of QPSK, 16-QAM and 64-QAM are shown in Figure 3.24 with zero, 3 and 5 percent gain mismatches.

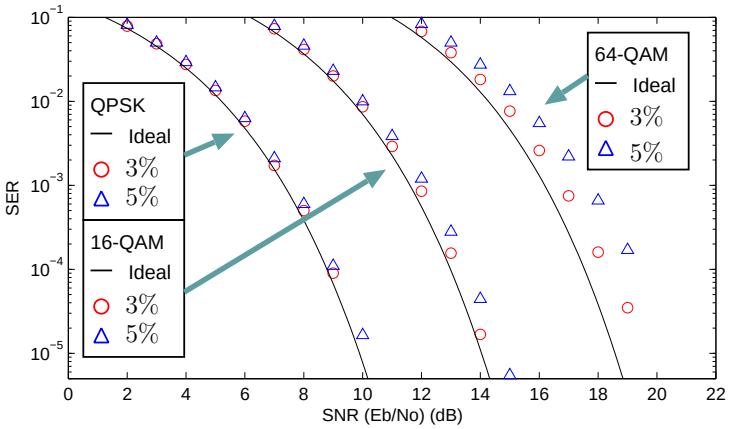


Figure 3.24. Simulated SER of the IEEE802.11a PHY link corrupted by the I, Q gain mismatch.

The gain mismatch problem has been a critical issue for designs using discrete components, and image-rejection receivers because of the IRR issue discussed in chapter 2. However for integrated implementations, the gain mismatch is much less troublesome, especially for direct downconversion receivers [2].

In addition to the gain mismatch, phases of the quadrature mixer also exhibit imbalance. As shown in Figure 3.25, the LO phase of the Q path has an error of θ, so the downconverted I and Q signals become

$$out_I = \frac{A}{2} I(t), \tag{3.21}$$

$$out_Q = \frac{A}{2}[Q(t)\cos(\theta) + I(t)\sin(\theta)]. \tag{3.22}$$

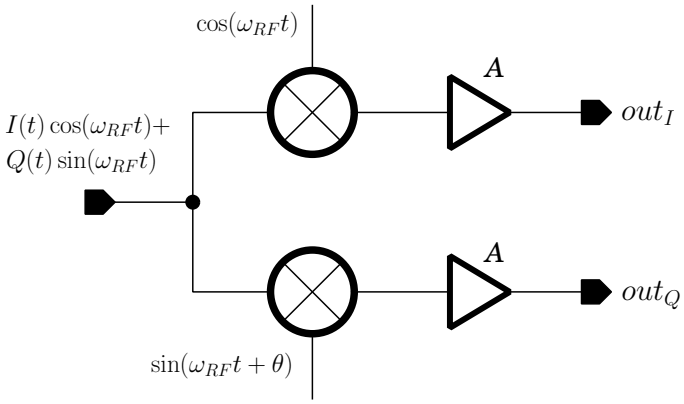


Figure 3.25. Downconversion with the I, Q phase mismatch.

From Eq. 3.22, the effect of phase error can be described as that the I channel signal corrupts the Q channel signal by a fraction of $(A/2)I(t)\sin(\theta)$, and a gain shrinkage of

$\cos(\theta)$ along the Q path. The effect of phase imbalance on a QPSK signal constellation is shown in Figure 3.26. Similar to the gain mismatch, along the I path, the energy contained in a single bit E_b remains the same, whereas along the Q path, the E_b appears unsymmetrical. Two diagonal symbols spread further and the other two move closer. Since the total gain along the Q path is shrunk by the factor $\cos(\theta)$, the E_b of the Q channel output is less than that of the ideal case, hence reduces the SER.

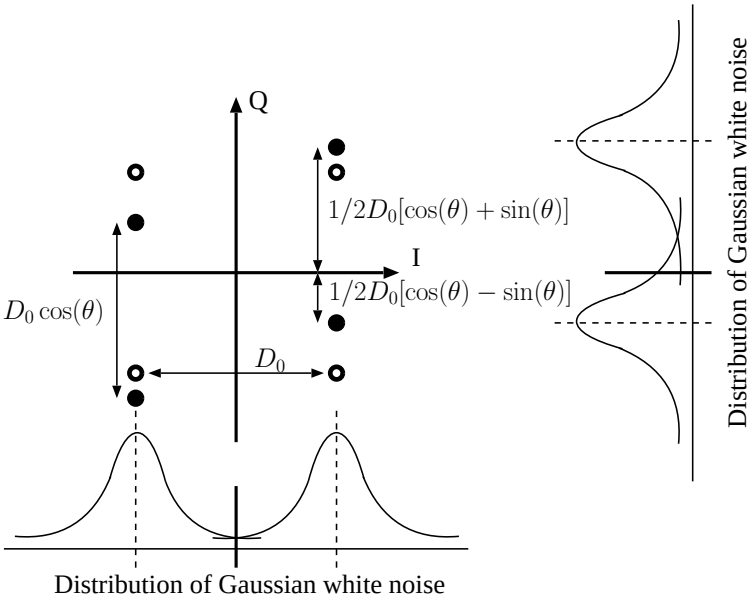


Figure 3.26. Effect of the quadrature phase mismatch on a QPSK signal.

The SIMULINK model for the SER simulation with phase mismatch is illustrated in Figure 3.27. The phase error is introduced according to Eq. 3.22. The SER simulation results are shown in Figure 3.28 with phase errors of zero, 3 and 5 degrees.

In an integrated receiver system, the phase mismatch issue also tends to decrease. However as shown in Figure 3.28 that high order QAM modulations are more sensitive to the phase mismatch. When 64-QAM modulation is utilised, the phase mismatch should not exceed 3 degrees, therefore the quadrature LO design becomes a crucial issue.

3.8 Summary

The physical link of IEEE802.11a standard utilising 64 channels OFDM modulation is introduced. The pulse shaping technique using raised-cosine filters for the better spectrum

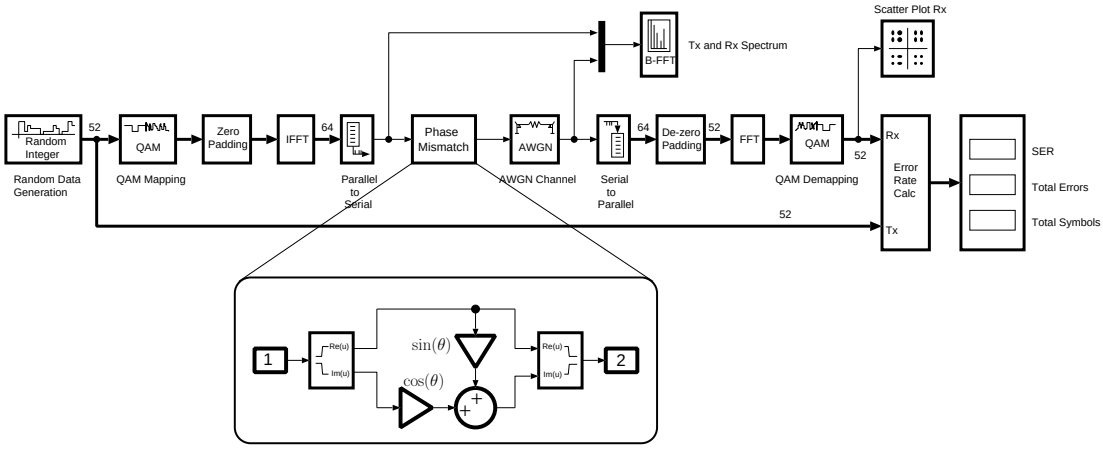


Figure 3.27. IEEE802.11a PHY link SIMULINK model for SER simulations corrupted by the phase mismatch.

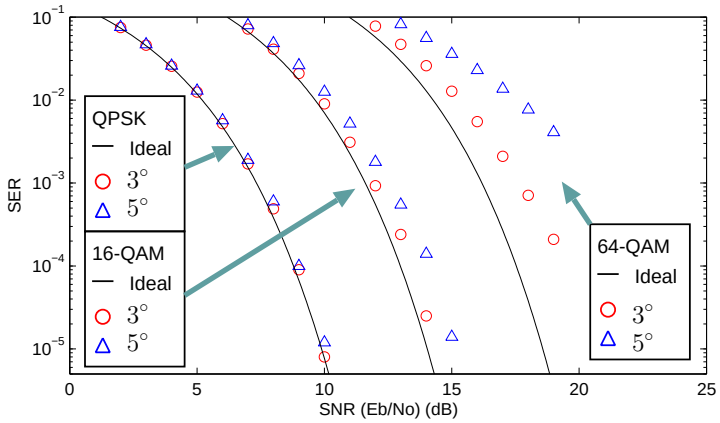


Figure 3.28. Simulated SER of the IEEE802.11a PHY link corrupted by the phase mismatch.

efficiency is discussed. A SIMULINK IEEE802.11a PHY model has been setup for the system level SER simulations with receiver non-idealities, including the highpass filtering, thermal noise, flicker noise, phase noise and the I, Q mismatches.

For direct downconversion receivers, there are no IF filtering and gain stages, so the receiver noise performance and the baseband circuitry linearity are critical. Quadrature mismatch issue is much less troublesome in highly integrated direct downconversion receivers. However, to achieve an acceptable SER, phase mismatch must be reduced when utilising 64-QAM modulation.

In the next chapter, the circuit level design of a direct downconversion receiver for the IEEE802.11a standard is presented. Circuit level design concerns, especially the noise related issues, are further discussed.

Chapter 4

Receiver Circuit Design

4.1 Introduction

As discussed at the system level, the direct downconversion architecture has advantages for the IEEE802.11a standard using OFDM technique. In this chapter, the circuit level design of a direct downconversion receiver operating at 5.25 GHz for IEEE802.11a WLAN applications is presented. The TSMC 0.18 µm RF CMOS process with a supply voltage of 1.8 V is used for the chip implementation.

The receiver frontend design is first introduced, including the LNA and mixer. The LNA design methodology is particularly focused, starting from the classic noise theory to the novel design methodology with good noise performance. The mixer conversion gain and flicker noise are analysed in detail, followed by a design example for the IEEE802.11a receiver. Next, the design of the baseband circuitry, including the VGA and the channel-selection filter, is presented. The OTA-C VGA architecture is chosen to meet the noise figure requirement at low frequencies. The design of a two-stage low voltage OTA for the VGA and the channel-selection filter is described. Simulations of each building block and the whole receiver at the circuit level using ADS2003 and HSPICE simulators are also presented.

4.2 From The Classic Two-Port Network Noise Theory to The LNA Design

4.2.1 The Classic Two-Port Network Noise Theory and The Noise Figure Prediction

Classic two-port noise theory has been introduced several decades ago [18] to simplify the noise analysis of complex circuits. As illustrated in Figure 4.1, a noisy two-port network can be represented as a noise-free network with a pair of external voltage noise source v_n and current noise source i_n. The input and output noise behaviour of the two-port network then can be evaluated together with the source admittance.

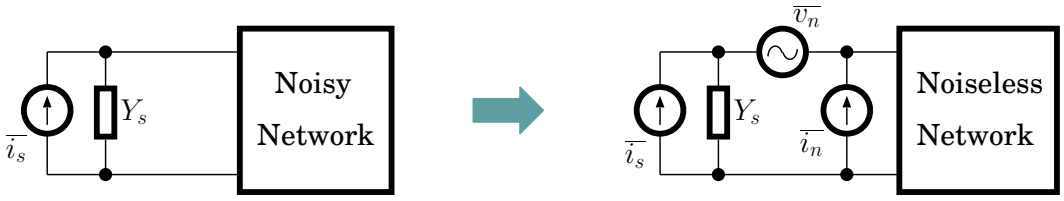


Figure 4.1. Two-port network noise approximation.

With this approximation, the noise factor F, defined as the total output noise power divided by the output noise power due to the input source, can be expressed as

$$F = 1 + \frac{\overline{|i_n + Y_s v_n|^2}}{\overline{i_s^2}}. \tag{4.1}$$

This formula is obtained with the assumption that the voltage and current noise sources are uncorrelated, which is not true in MOS transistors. In fact, the two noise sources are partially correlated. For the inclusion of the partial correlation between the two noise sources, i_n is separated into an uncorrelated component i_{nu} and a completely correlated component i_{nc} expressed as

$$i_{cn} = Y_c v_n, \tag{4.2}$$

where Y_c is the correlation admittance. Substituting Eq. 4.2 into Eq. 4.1 gives the noise factor with partially correlated noise sources as

$$F = 1 + \frac{\overline{i_{nu}^2} + |Y_s + Y_c|^2 \overline{v_n^2}}{\overline{i_s^2}}. \tag{4.3}$$

Representing the noise sources in terms of equivalent resistance or conductance, the noise factor F can be further expressed as

$$F = 1 + \frac{G_u + \left[(G_c + G_s)^2 + (B_c + B_s)^2\right] R_n}{G_s}, \tag{4.4}$$

where

$$Y_s = G_s + jB_s, \tag{4.5}$$

$$Y_c = G_c + jB_c \tag{4.6}$$

$$R_n = \frac{\overline{v_n^2}}{4kT\Delta f}, \tag{4.7}$$

$$G_u = \frac{\overline{i_u^2}}{4kT\Delta f}, \tag{4.8}$$

$$G_s = \frac{\overline{i_s^2}}{4kT\Delta f}. \tag{4.9}$$

Solving $\partial F/\partial G_s = 0$ and $\partial F/\partial B_s = 0$ for the minimum noise factor F gives the optimised source admittance as

$$B_{opt} = -B_c, \tag{4.10}$$

$$G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2}; \tag{4.11}$$

and the minimum noise factor is then given by

$$F_{min} = 1 + 2R_n \left[\sqrt{\frac{G_u}{R_n} + G_c^2} + G_c\right]. \tag{4.12}$$

Using Eqs. 4.10, 4.11 and 4.12, the noise factor can be simplified as

$$F = F_{min} + \frac{R_n}{G_s}\left[(G_s - G_{opt})^2 + (B_s - B_{opt})^2\right]. \tag{4.13}$$

The expressions in Eq. 4.12 and Eq. 4.13 are so-called classic two-port network noise theory, which can be found in most of the noise related materials.

A useful application of the classic two-port network noise theory is to predict the minimum MOSFET noise figure. A CS connected MOSFET with noise sources including the source thermal noise $\overline{i_{ns,in}^2}$, the channel thermal noise $\overline{i_{nd,in}^2}$, and the gate induced noise $\overline{i_{ng,in}^2}$ is shown in Figure 4.2. The three noise sources are given by

$$\overline{i_{ns,in}^2} = 4kTG_s, \tag{4.14}$$

$$\overline{i_{nd,in}^2} = 4kTg_m\frac{\gamma}{\alpha}, \tag{4.15}$$

$$\overline{i_{ng,in}^2} = 4kT\delta\frac{\alpha\omega^2 C_{gs}^2}{5g_m}, \tag{4.16}$$

where g_m is the transconductance of the MOSFET, C_{gs} is the parasitic gate capacitance and α, γ, δ are the noise parameters. For long channel transistors in the saturation region, those parameters have been verified as $\alpha = 1$, $\gamma = 2/3$ and $\delta = 2\gamma = 4/3$ [12]. For short channel MOSFETs, the exact physical model of those parameters are still not clear yet, and hence no fixed value have been reported in the literature [13]. If the noise sources are still expressed using the long channel formulas, then α can be shrink to 0.6 or even smaller and γ can be greater than 2 [13]. For the gate induced noise parameter δ, we still expect it as double as γ [13], thereby can be greater than 4. This is because the gate induced noise and the channel thermal noise follow the same mechanism, hence although the exact value is still uncertain, the ratio between δ and γ is possible to remain the same. For all the numerical calculations in this chapter, targeted for the implementation using TSMC 0.18 µm CMOS process, α, γ, δ are chosen as 0.6, 2 and 4 respectively. For simplicity, the bandwidth for the noise power measurement is set to 1 Hz, thereby the term of Δf in each noise formula is removed; or it can be interpreted as the noise power spectrum density.

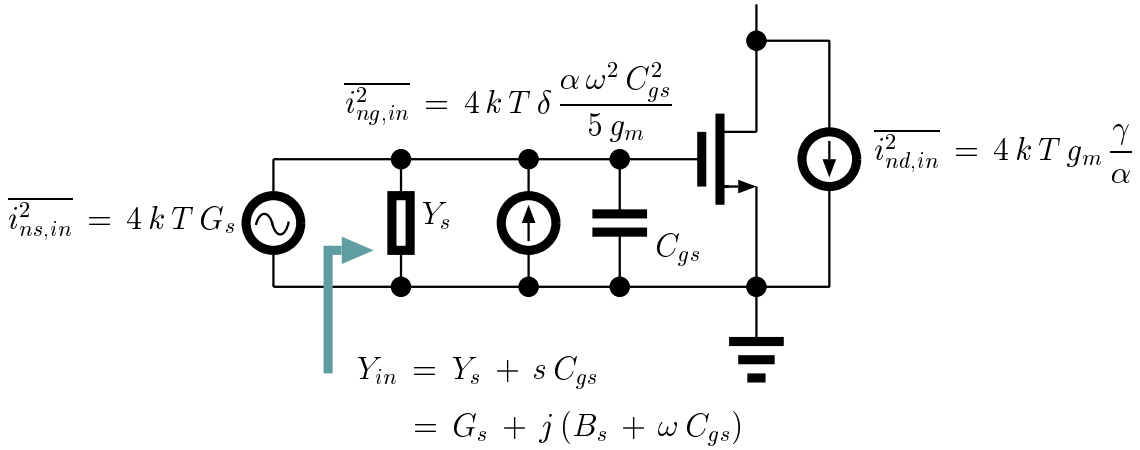


Figure 4.2. MOSFET minimum noise figure prediction

From Figure 4.2, because of the parallel connection of the source admittance and the parasitic gate capacitor, the equivalent input admittance is given by

$$Y_{in} = G_s + j(B_s + \omega C_{gs}). \tag{4.17}$$

With Eq. 4.17 in hand, since the output current $i_{out} = g_m V_g$, where V_g is the MOSFET gate voltage, all the noise sources presented at the transistor output can be derived as

$$i_{ns,out} = \frac{g_m}{G_s + j(\omega C_{gs} + B_s)} i_{ns,in}, \tag{4.18}$$

$$i_{nd,out} = i_{nd,in}, \tag{4.19}$$

$$i_{ng,out} = \frac{g_m}{G_s + j(\omega C_{gs} + B_s)} i_{ng,in}. \tag{4.20}$$

The noise figure of the CS MOSFET can be written using Eqs. 4.18∼4.20 as

$$F = 1 + \frac{\overline{|i_{nd,out} + i_{ng,out}|^2}}{\overline{i^2_{ns,out}}}. \tag{4.21}$$

Because $i_{nd,out}$ and $i_{ng,out}$ are partially correlated, the numerator in Eq. 4.21 is therefore expanded as

$$\overline{|i_{nd,out} + i_{ng,out}|^2} = \overline{i_{nd,out} i^*_{nd,out}} + \overline{i_{ng,out} i^*_{nd,out}} + \overline{i^*_{ng,out} i_{nd,out}} + \overline{i_{ng,out} i^*_{nd,out}}, \tag{4.22}$$

where the last two terms represent the correlated noise contribution. To further discuss the correlated noise terms, a correlation noise coefficient is defined as

$$c = \frac{\overline{i_{ng,in} i^*_{nd,in}}}{\sqrt{\overline{i_{ng,in} i^*_{ng,in}} \times \overline{i_{nd,in} i^*_{nd,in}}}}. \tag{4.23}$$

For long channel transistors c is calculated as $0.395j$ [13], but unknown in the short channel regime. Since the gate induced noise and the channel thermal noise share the same mechanism, this value is also assumed the same for short channel transistors [13]. Using Eqs. 4.19, 4.20 and 4.23, the correlated noise terms are then derived as

$$\overline{i_{ng,out} i^*_{nd,out}} = \overline{i^*_{ng,out} i_{nd,out}} = j|c| A_I^2 \sqrt{\overline{i_{ng,in} i^*_{ng,in}} \times \overline{i_{nd,in} i^*_{nd,in}}}, \tag{4.24}$$

where

$$A_I = \frac{g_m}{G_s + j(\omega C_{gs} + B_s)} \tag{4.25}$$

is the current gain. Substituting Eq. 4.22, 4.24 and 4.25 into Eq. 4.21 yields the noise factor as

$$F = 1 + \frac{\alpha \delta \omega^2_{RF} C^2_{gs}}{5 g_m G_s} + \frac{\gamma}{\alpha g_m G_s} \left[(g_m + G_s)^2 + (\omega C_{gs} + B_s)^2 \right] + 2|c| \sqrt{\frac{\delta \gamma}{5}} \frac{\omega C_{gs}}{g_m G_s} (\omega C_{gs} + B_s). \tag{4.26}$$

Following the classic two-port network noise theory, solving $\partial F/\partial G_s = 0$ and $\partial F/\partial B_s = 0$ for the minimum noise factor F gives the optimised source admittance as

$$G_{sopt} = \sqrt{\alpha^2\omega^2 C_{gs}^2 \frac{\delta}{5\gamma}(1-|c|^2)}, \tag{4.27}$$

$$B_{sopt} = -\omega C_{gs}\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right), \tag{4.28}$$

and the corresponding minimum noise figure is then given by

$$F_{min} = 1 + 2\sqrt{\frac{\gamma\delta}{5}}\frac{\omega}{\omega_T}\sqrt{(1-|c|^2)+\frac{\gamma}{5\delta}\left(\frac{\omega}{\omega_T}\right)^2} + \frac{2\gamma}{5}\left(\frac{\omega}{\omega_T}\right)^2, \tag{4.29}$$

where $\omega_T = g_m/C_{gs}$ is the MOSFET unity current gain frequency in radians. The final results of Eqs. 4.27∼4.29 are identical to those derived in [13], but from a different approach.

Eq. 4.29 is plotted in Figure 4.3 with two RF frequencies at 2.4 GHz and 5.25 GHz. The plot shows that the larger ω_T the better noise figure. For TSMC 0.18 µm CMOS process, assuming L=0.2 µm, I_{ds}=5 mA and C_{ox}=8.57e-3 m^2/F, f_T is then calculated as 58 GHz. The corresponding minimum noise figures at f_{RF}=2.4 GHz and f_{RF}=5.25 GHz are 0.4 dB and 0.8 dB, respectively.

The classic two-port noise theory and the minimum noise figure prediction do provide an insight into the noise factor analysis together with the source impedance. However, "is this theory useful for the integrated LNA design?" It is clear that this theory seems to optimise the source impedance to match a given amplifier. On the other hand, the source impedance in an RF system is usually the standard 50 ohm. This requires the noise optimisation relying on the amplifier design with respect to the device characteristics, such as transistor length, width and channel current etc, to match the 50 ohm source impedance. The classic noise theory gives the opposite way for the noise optimisation, and therefore an alternative approach for the noise optimisation is required.

4.2.2 V_{od} and I_{ds} constrained LNA Design Methodologies

CS LNAs are widely used in wireless receivers when the radio frequency is much smaller than the transistor ω_T. A typical CS LNA is illustrated in Figure 4.4. CS connected M_1

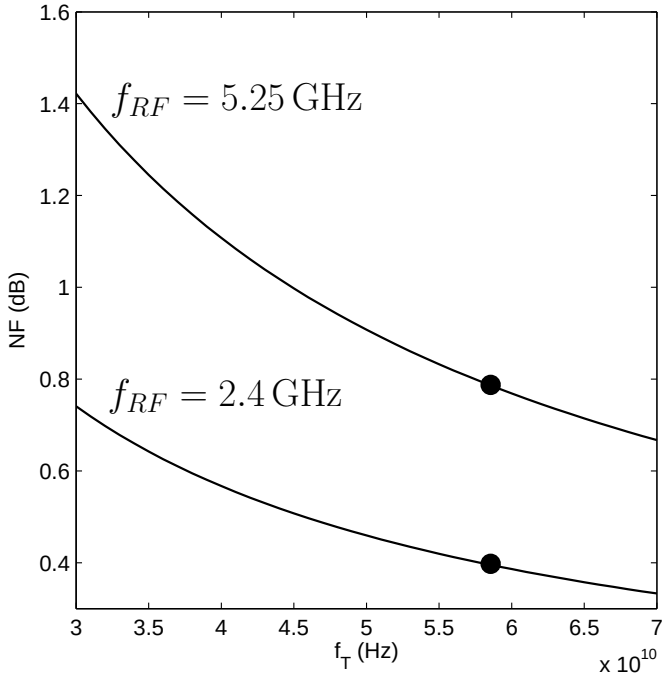


Figure 4.3. MOSFET minimum noise figures Vs. f_T at 2.4 GHz and 5.25 GHz.

is the gain stage; CG connected M_2 isolates the output and the input ports to improve the S_{12}; M_3 and M_1 form a current mirror that biases the amplifier. The gate inductor L_g and the source inductor L_s achieve the impedance matching when the dimension and the current bias of M_1 are determined. R_{L_g} is the parasitic resistor of the gate inductor L_g. The LC tank acts as the LNA load, having a resonant frequency of the carrier signal.

From the schematic, the LNA equivalent input impedance can be written as

$$Z_{in} = sL_s + sL_g + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}}. \tag{4.30}$$

When the impedance matching is satisfied at the RF, Z_{in} is equal to the conjugated source impedance R_s^*, which is usually 50 ohm. Therefore, the real and imaginary parts of the input impedance have the constrains of

$$sL_s + sL_g + \frac{1}{sC_{gs}} = 0, \tag{4.31}$$

$$\frac{g_m L_s}{C_{gs}} = R_s. \tag{4.32}$$

Demonstrating on the Smith-Chart, the source and the LNA input impedance can be matched by first tuning L_s to make the S_{11} curve on the unity normalised resistance

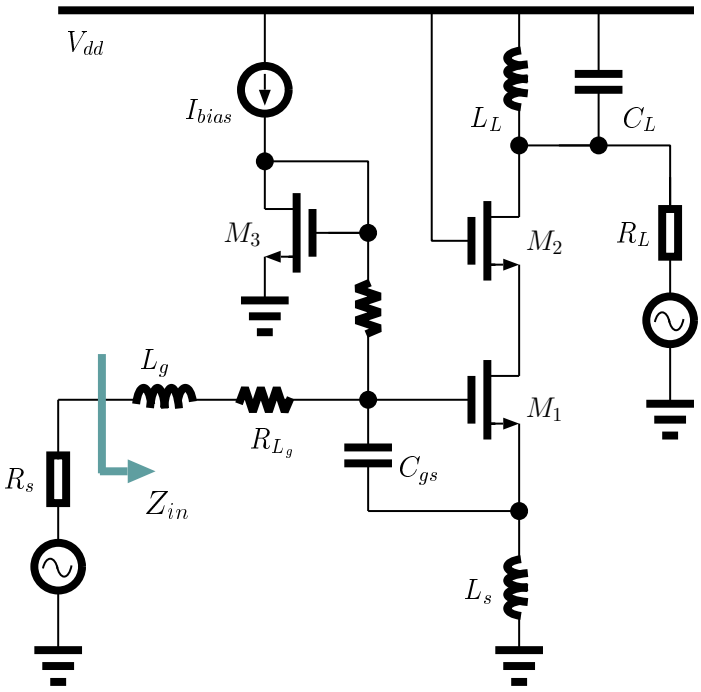


Figure 4.4. Schematic of a CS LNA.

circle and then tuning L_g to make the resonant frequency at the RF, as illustrated in Figure 4.5.

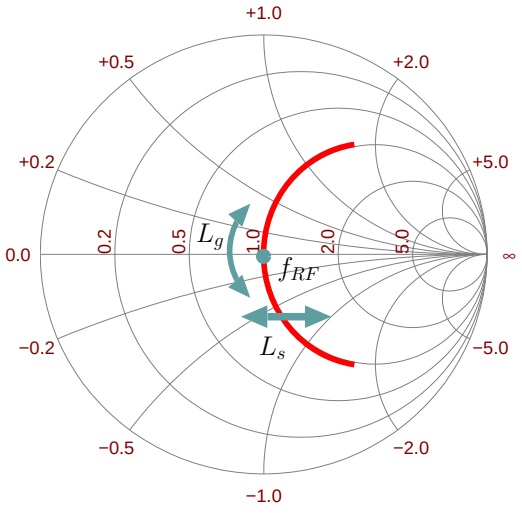


Figure 4.5. LNA impedance matching by L_g and L_s tuning.

The noise sources introduced at the output of M_1 are much less critical because the RF signal has been amplified. The important noise sources are associated with the

components of the input stage. The LNA input stage for noise analysis is shown in Figure 4.6. Four noise sources are considered: (1) the input source thermal noise $\overline{v_{ns,in}^2}$, (2) the channel thermal noise $\overline{i_{nd,in}^2}$, (3) the gate induce noise $\overline{i_{ng,in}^2}$, and (4) the thermal noise $\overline{v_{nR_{L_g},in}^2}$ of the parasitic resistor R_{L_g} of L_g. At the input of the LNA, the four noise sources can be expressed as:

$$\overline{v_{ns,in}^2} = 4kTR_s, \tag{4.33}$$

$$\overline{i_{nd,in}^2} = 4kTg_m\frac{\gamma}{\alpha}, \tag{4.34}$$

$$\overline{i_{ng,in}^2} = 4kT\delta\frac{\alpha\omega^2C_{gs}^2}{5g_m}, \tag{4.35}$$

$$\overline{v_{nR_{L_g}}^2} = 4kTR_{L_g}. \tag{4.36}$$

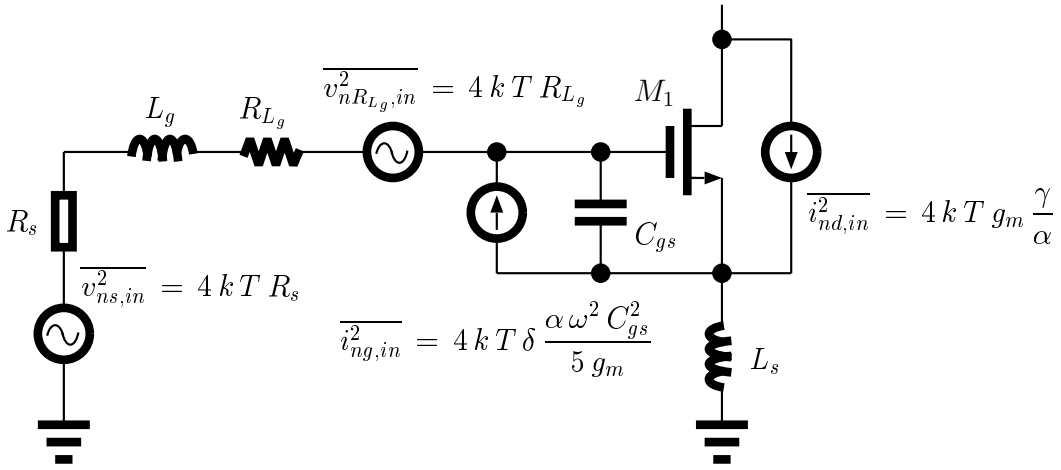


Figure 4.6. Input stage of the CS LNA for the noise figure calculation.

In order to calculate the noise at the output of M_1, it is convenient to introduce an equivalent transconductance of the LNA, including M_1, the matching network L_g and L_s, and the source resistor R_s. Reflecting M_1 output current as an input voltage across C_{gs} gives

$$\begin{aligned} G_m &= \frac{g_m}{\omega_{RF}C_{gs}(R_s+\omega_T L_s)} \\ &= \frac{\omega_T}{2\omega_{RF}R_s} \\ &= Q_{in}g_m, \end{aligned} \tag{4.37}$$

where $Q_{in} = 1/2R_s\omega_{RF}C_{gs}$ is the effective Q factor of the LNA input stage. The second equality takes the impedance matching constrains given in Eqs. 4.31 and 4.32. Q_{in} and C_{gs}

are interdependent, hence only one of them can be freely controlled. With the equivalent G_m in hand, the uncorrelated noise components at the output node can be calculated as

$$\overline{i_{ns,out}^2} = G_m^2 \cdot \overline{v_{nd,in}^2}, \tag{4.38}$$

$$\overline{i_{nR_{Lg},out}^2} = G_m^2 \cdot \overline{v_{nR_{Lg}}^2}, \tag{4.39}$$

$$\overline{i_{nd,out}^2} = \frac{1}{4} \cdot \overline{i_{nd,in}^2}, \tag{4.40}$$

$$\overline{i_{ng,out}^2} = \frac{1}{4} \cdot \left(\frac{g_m}{\omega_{RF} C_{gs}}\right)^2 \left[1 + \frac{1}{R_s^2 \omega_{RF}^2 C_{gs}^2}\right] \cdot \overline{i_{ng,in}^2}. \tag{4.41}$$

Besides the output channel thermal noise and the gate induced noise given by Eqs. 4.40 and 4.41 respectively, there is still a correlated component between the two. Rewriting the output channel thermal noise and the gate induced noise as

$$i_{nd,out} = \frac{1}{2} \cdot i_{nd,in}, \tag{4.42}$$

$$i_{ng,out} = \frac{g_m}{j\omega_{RF} C_{gs}} \cdot \frac{j\omega_{RF} R_s C_{gs} - 1}{j\omega_{RF} C_{gs}} \cdot i_{ng,in}, \tag{4.43}$$

and with the help of the correlation coefficient c from Eq. 4.23, the correlated term can be derived as

$$\begin{aligned}
\overline{i_{nc,out}^2} &= \overline{i_{ng,out} i_{nd,out}^*} + \overline{i_{ng,out}^* i_{nd,out}} \\
&= \frac{j|c|}{2} \left[\frac{g_m}{j\omega_{RF} C_{gs}} \cdot \frac{j\omega_{RF} R_s C_{gs} - 1}{j\omega_{RF} C_{gs}} - \left(\frac{g_m}{j\omega_{RF} C_{gs}} \cdot \frac{j\omega_{RF} R_s C_{gs}}{j\omega_{RF} C_{gs}}\right)^*\right] \cdot \sqrt{\overline{i_{ng,in}^2} \cdot \overline{i_{nd,in}^2}} \\
&= \frac{|c| g_m}{2\omega_{RF} C_{gs}} \sqrt{\overline{i_{ng,in}^2} \cdot \overline{i_{nd,in}^2}}.
\end{aligned} \tag{4.44}$$

According to the definition, the noise factor of the LNA can be presented as

$$F = 1 + \frac{\overline{i_{nd,out}^2} + \overline{i_{ng,out}^2} + \overline{i_{nc,out}^2} + \overline{i_{nR_{Lg},out}^2}}{i_{ns,out}^2}. \tag{4.45}$$

Substituting Eqs. 4.38∼4.41 and Eq. 4.44 into Eq. 4.45, and after some simplification yields

$$F = 1 + \frac{\alpha\delta}{5R_s g_m} + \frac{\alpha\delta R_s \omega_{RF}^2 C_{gs}^2}{5g_m} + \frac{\gamma R_s \omega_{RF}^2 C_{gs}^2}{\alpha g_m} + 2|c|\sqrt{\frac{\gamma\delta}{5}} \frac{R_s \omega_{RF}^2 C_{gs}^2}{g_m} + \frac{R_{Lg}}{R_s}. \tag{4.46}$$

The noise factor is a function of two dependent variables, the MOSFET transconductance g_m and the gate parasitic capacitor C_{gs}. In order to have two independent parameters, g_m can be replaced by

$$g_m = \frac{3}{2} \frac{\mu_0}{1 + \theta V_{od}} \frac{C_{gs}}{L^2} V_{od}, \tag{4.47}$$

where $V_{od} = V_{gs} - V_{th}$ is the gate overdrive voltage, L is the MOSFET channel length, which usually is chosen as the minimum value for high ω_T, and θ models the mobility degradation and the velocity saturation due to the vertical and lateral electrical field respectively in a short channel MOS transistor. As an estimation, θ can be obtained from $2 \times 10^{-9}/T_{ox}$ [13], where T_{ox} is the gate oxide thickness. For TSMC 0.18 µm CMOS process, θ is calculated as 0.498 for the numerical analysis in this chapter.

Substituting Eq. 4.47 into Eq. 4.46, the noise factor can be represented as a function of two independent parameters C_{gs} and V_{od}:

$$F = f(C_{gs},\ V_{od}), \tag{4.48}$$

where

$$C_{gs} = \frac{2}{3} W L C_{ox} \tag{4.49}$$

links the device dimension, and V_{od} is related to ω_T and the power dissipation. The minimum noise factor F can be obtained by solving Eq. 4.48 as a function of C_{gs} at a fixed value of V_{od}. This approach can be referred to as the V_{od} constrained optimisation.

The calculated noise figures at 2.4 GHz with different values of V_{od} are shown in Figure 4.7. For simplicity, R_{L_g} is neglected. The larger V_{od}, which translates to a higher ω_T, results in a better noise figure. However, this is somewhat artificial because V_{od} and ω_T cannot be arbitrarily large as the transistor must be properly biased in the saturation region and ω_T is limited by the fabrication process.

The V_{od} constrained optimisation gives very large transistor size, about 367 µm for a 0.18 µm CMOS process. The corresponding bias current for each V_{od} is also shown in Figure 4.7. To achieve the minimum noise figure at 2.4 GHz, about 0.42 dB calculated by Eq. 4.29, the overdrive voltage V_{od} should be 0.3V, resulting in a drain current of 30 mA.

Another feature of V_{od} constrained optimisation is that the noise figure becomes flat when C_{gs} is greater than 0.3 pF. This means that the noise figure is insensitive to the device dimension when the device and bias current are large enough. This validates the common understanding: large devices with large bias current result in good noise performance. This understanding could be useful for some receiver design, where the power dissipation is not a critical issue; but for mobile wireless systems, such a large bias current will significantly degrade the power performance.

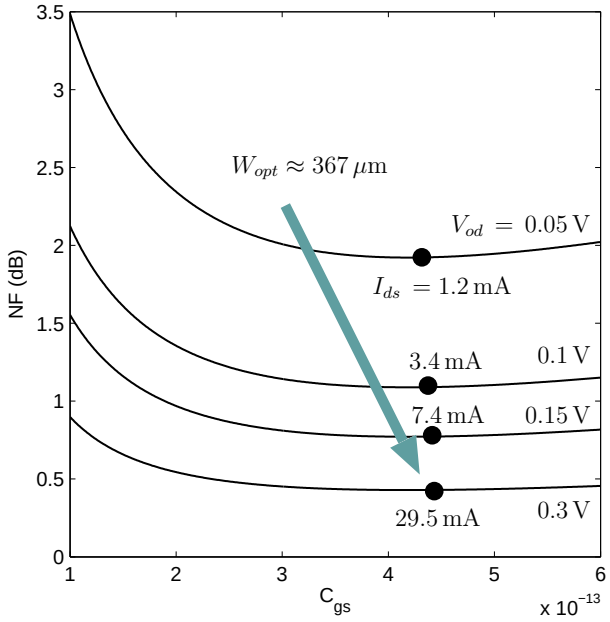


Figure 4.7. V_{od} constrained noise figure optimisations at 2.4 GHz.

In order to achieve a reasonable power dissipation, noise performance may be sacrificed by reducing the gate overdrive voltage V_{od}. However, this may cause another design challenge, linearity. To analyse the LNA linearity, the output current of M_1 is written as

$$I_{ds} = \frac{3C_{gs}}{4L^2}\frac{\mu_0}{1+\theta(V_{od}+V_{ac})}(V_{od}+V_{ac})^2, \tag{4.50}$$

where V_{ac} is the AC input signal. When V_{ac} contains two sinusoid signals with different frequencies, the IIP3 point can be approximated as [3]

$$IIP3^2 \approx \frac{3}{4}\left|\frac{G_1}{G_3}\right|, \tag{4.51}$$

where G_1 and G_3 are the transconductance of the fundamental and the third-order harmonic tones. Expanding Eq. 4.50 in Taylor series as a function of V_{ac} and substituting the first and third order transconductance into Eq. 4.51 results in the IIP3 point as

$$IIP3^2 \approx \frac{4}{3}\frac{V_{od}(2+\theta V_{od})(1+\theta V_{od})^2}{\theta}. \tag{4.52}$$

As shown in Eq. 4.52, the IIP3 improves along with V_{od}, so it is not desired to control the power dissipation by reducing the gate overdrive voltage, especially for a large MOS transistor given by the V_{od} constrained design methodology. As for a fixed bias current, a larger transistor results in smaller V_{od}, hence linearity reduction.

Another approach of the noise factor formula is to use the bias current I_{ds}. In Eq. 4.50, removing the AC signal V_{ac} and representing V_{od} by I_{ds} gives

$$V_{od} = \frac{2I_{ds}L^2\theta + 2L\sqrt{I_{ds}^2L^2\theta^2 + 3\mu_0 C_{gs} I_{ds}}}{3\mu_0 C_{gs}}. \tag{4.53}$$

Substituting Eq. 4.53 into Eq. 4.47 to replace V_{od} by I_{ds}, and substituting the g_m expression into Eq. 4.46, the noise factor becomes a function of C_{gs} and I_{ds} as

$$F = f(C_{gs},\ \ I_{ds}), \tag{4.54}$$

where C_{gs} is related to the device dimension, and I_{ds} is related to the power consumption and ω_T. With a fixed value of I_{ds} and solving Eq. 4.54 for the minimum noise factor as a function of C_{gs} yields the I_{ds} constrained optimisation.

The calculated noise figures at 2.4 GHz are shown in Figure 4.8 with different values of I_{ds}. Each optimised C_{gs} is much smaller than that of the V_{od} constrained design. For 5 mA bias current, the optimised MOSFET width is about 217 µm and the corresponding noise figure is about 0.82 dB. This result is very close to the optimised transistor width given by the well-known power constrained design [19] as

$$\begin{aligned} W_{opt,P_D} &= \left[\frac{2}{3}\omega_{RF} L C_{ox} R_s Q_{opt,P_D}\right]^{-1} \\ &= 232\mu m, \end{aligned} \tag{4.55}$$

where Q_{opt,P_D} is equal to 5.0 for 9 mW power consumption (5 mA$\times$ 1.8 V), although more sophisticated g_m formula is employed for the derivation of Eq. 4.55.

Recall the minimum noise figure prediction of 0.42 dB given by Eq. 4.29, the I_{ds} and power constrained design methodologies sacrifice the noise figure by double the value in decibel for a reasonable power dissipation.

4.2.3 (I_{ds}, Q_{in}) Constrained Design Methodology

The bridge that connects the noise performance of M_1 and its device dimension is the gate capacitor C_{gs}. In the previous design methodologies, the total gate capacitance for the noise matching is all introduced by C_{gs}, however this should not be the only choice.

As illustrated in Figure 4.9, the total M_1 gate capacitor C_{tot} can be split into two components: C_{gs}, which still links to the device dimension, and C_{ext}, an extra capacitor

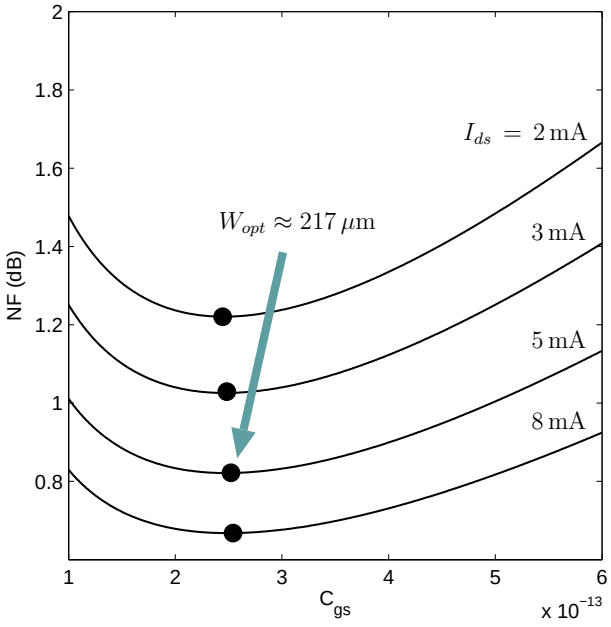


Figure 4.8. I_{ds} constrained noise figure optimisations at 2.4 GHz.

that introduces a degree of freedom. This extra gate capacitor is first introduced in [20] and also presented in [21] for the better impedance matching including the bonding-pad parasitics. For the (I_{ds}, Q_{in}) constrained design methodology, the total gate capacitor C_{tot} achieves the noise matching, whereas only part of the C_{tot} is turned into the transistor size. Therefore a smaller transistor is obtained and a better linearity is expected when the LNA drains the same current.

Using Eq. 4.37, the equivalent transconductance of the input stage now becomes

$$G_m = \frac{g_m}{2R_s C_{tot}\omega_{RF}} = Q_{in} g_m, \tag{4.56}$$

where Q_{in} is redefined as

$$\begin{aligned} Q_{in} &= \frac{1}{2R_s C_{tot}\omega_{RF}} \\ &= \frac{1}{2R_s (C_{gs} + C_{ext})\omega_{RF}}. \end{aligned} \tag{4.57}$$

With the extra degree of freedom introduced by the capacitor C_{ext}, Q_{in} can be treated as an independent parameter.

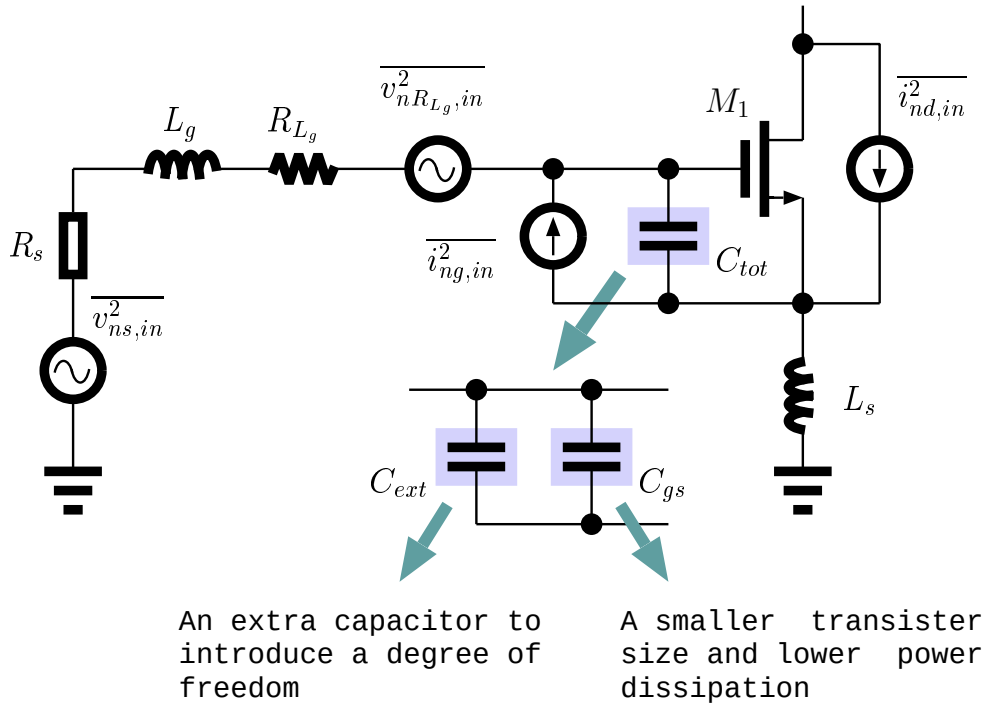


Figure 4.9. LNA input stage with an extra gate capacitor C_{ext}.

Following the same procedure for the derivation of Eq. 4.46, all the noise sources presented at the output can be expressed as:

$$\overline{i^2_{ns,out}} = G_m^2 \cdot \overline{v^2_{nd,in}}, \tag{4.58}$$

$$\overline{i^2_{nR_{L_g},out}} = G_m^2 \cdot \overline{v^2_{nR_{L_g}}}, \tag{4.59}$$

$$\overline{i^2_{nd,out}} = \frac{1}{4} \cdot \overline{i^2_{nd,in}}, \tag{4.60}$$

$$\overline{i^2_{ng,out}} = \frac{1}{4} \cdot \left(\frac{g_m}{\omega_{RF} C_{gs}}\right)^2 \left[1 + \frac{1}{R_s^2 \omega_{RF}^2 C_{gs}^2}\right] \cdot \overline{i^2_{ng,in}}, \tag{4.61}$$

and the noise factor is then calculated as

$$F = 1 + \frac{\alpha\delta\left(Q_{in}^2 + 1/4\right) C_{gs}^2}{5 R_s Q_{in}^2 g_m C_{tot}^2} + \frac{\gamma}{\alpha R_s Q_{in}^2 g_m} + 2|c|\sqrt{\frac{\delta\gamma}{5}} \frac{C_{gs}}{R_s Q_{in}^2 g_m C_{tot}} + \frac{R_{L_g}}{R_s}. \tag{4.62}$$

Making use of Eq. 4.57, C_{tot} can be written as

$$C_{tot} = \frac{1}{2 R_s Q_{in} \omega_{RF}}. \tag{4.63}$$

Substituting Eq. 4.49 and Eq. 4.63 into Eq. 4.62 results in the noise factor that is a function of three independent parameters as

$$F = f(W,\ I_{ds},\ Q_{in}), \tag{4.64}$$

where W is the MOSFET channel width, I_{ds} is related to the power dissipation and ω_T, and Q_{in} is the equivalent Q-factor of the input stage.

The calculated noise figures as a function of W with different values of Q_{in} are shown in Figure 4.10, using a bias current I_{ds} of 5 mA. The larger Q_{in} results in a smaller transistor size and a better noise figure. This is because for a fixed bias current, a smaller transistor width, hence smaller C_{gs}, results in a larger ω_T, and thereby a better noise performance.

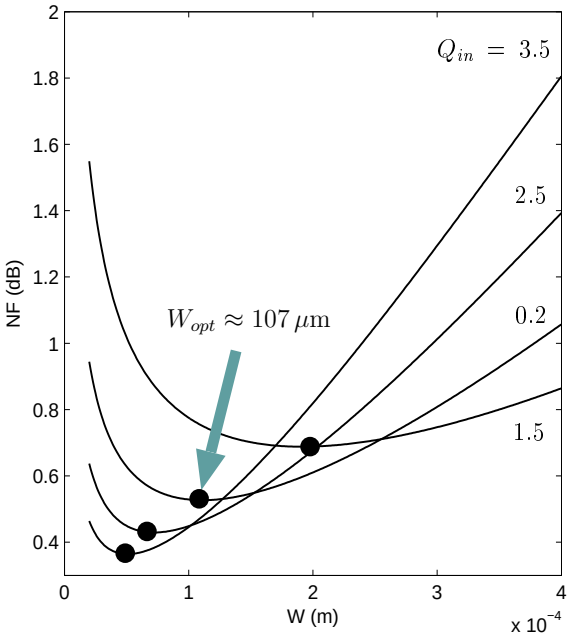


Figure 4.10. (I_{ds}, Q_{in}) constrained noise figure optimisations at 2.4 GHz.

To achieve the minimum noise figure of 0.42 dB predicted by Eq. 4.29, Q_{in} is chosen as 2.5 and the corresponding transistor width is 73 µm, as illustrated in Figure 4.10. However, this is somewhat artificial. In reality, ω_T does not always keep increasing with the shrinkage of the transistor width, but is limited by the fabrication process. A small C_{tot} requires a large gate inductor L_g to resonant at the RF, but a large inductor is difficult to achieve a good Q-factor, thereby the associated large parasitic resistance R_{L_g} degrades the noise figure. In practise, an achievable LNA noise figure calculated by the (I_{ds}, Q_{in}) constrained methodology relies on a reasonable Q_{in} value. With the cooperation of EDA

simulations, it shows that Q_{in}=2 is a good initial value for the prototype design of a multi-gigahertz LNA using the TSMC 0.18 µm RF CMOS process.

[Example 4.1: A 2.4 GHz LNA] For 2.4 GHz applications, assuming $Q_{in} = 2$, the noise figure as a function of transistor width W is plotted in Figure 4.11. The effect of the parasitic gate resistor R_{L_g} of L_g is included. When L_g is realised using bonding wire inductor, the length of the bonding wire inductance per unit length is given by 1 nH/mm and the parasitic R_{L_g} is given by 0.1 ohm/mm. The optimised channel width W is about 107 µm and the corresponding noise figure is 0.62 dB. The source degeneration and the gate inductance are calculated as 0.38 nH and 12.8 nH respectively, and the extra capacitor C_{ext} is 0.21 pF. □

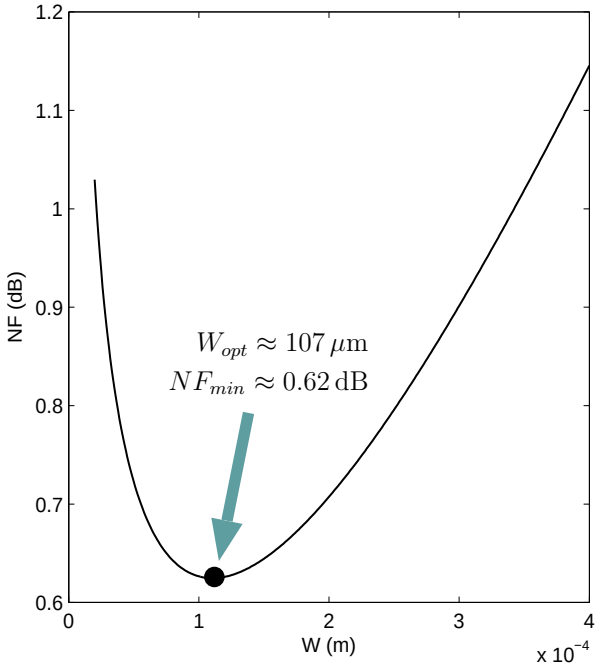


Figure 4.11. (I_{ds}, Q_{in}) constrained noise figure optimisation of a 2.4 GHz LNA.

[Example 4.2: A 5.25 GHz LNA] For 5.25 GHz applications, to avoid a too small transistor, Q_{in} is set to 1.7. The noise figure as a function of the transistor width W is shown in Figure 4.12. The optimised channel width W is about 70 µm and the corresponding noise figure is 0.93 dB. The source degeneration and the gate inductance are 0.27 nH and 4.9 nH respectively. The C_{ext} is calculated as 0.1 pF. □

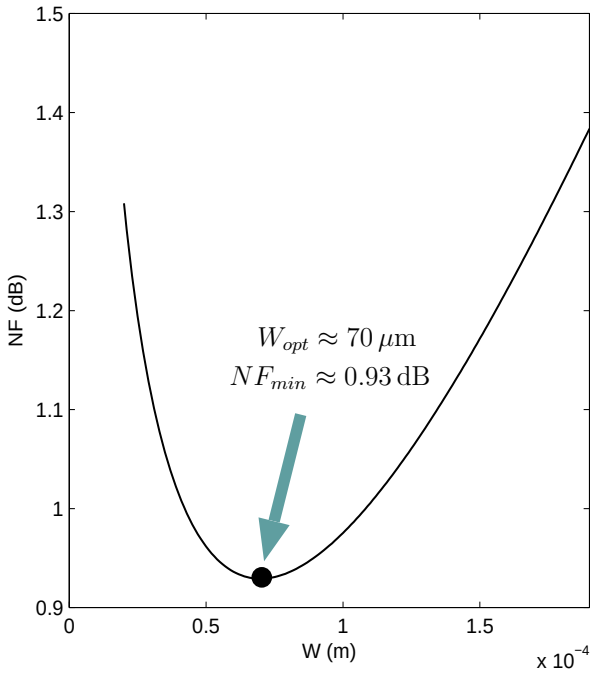


Figure 4.12. (I_{ds}, Q_{in}) constrained noise figure optimisation of a 5.25 GHz LNA.

The LNA schematic using the TSMC 0.18 µm RF CMOS process is shown in Figure 4.13 with the subcircuits of the RF MOSFET and the on-chip spiral inductor. The enhanced thermal noise for short channel transistors and the gate noise are captured by the passive components shown in the MOSFET subcircuit. The gate and source inductors are realised using bonding wires. The parasitic resistance associated with the bonding wire inductor is given by 0.1 ohm/mm. In order to avoid too small source inductance, a pair of bonding wire inductors are used with double the value of L_s. C_{o1}, C_{o2} and L_o are for the output impedance matching. The detailed device parameters of the 2.4 GHz and the 5.25 GHz LNAs are listed in Table 4.1, and the simulation results are presented in Table 4.2. The RF frequencies for the IIP3 simulations are 2.405/2.406 GHz for the 2.4 GHz LNA and 5.255/5.256 GHz for the 5.25 GHz LNA.

The extra capacitor C_{ext} is formed by the bond-pad metal layers as illustrated in Figure 4.14. The metal layers 1∼4 are connected and grounded. This ground shield avoids the signal power loss and the extra noise due to the substrate coupling [22]. The gate and source are connected to the metal layers 6 and 5 respectively, so that the capacitors between metal layers 6, 5 and layers 5, 4 realise the C_{ext} and C_s. The size of the bond-pad

		2.4 GHz	5.25 GHz
M_1, M_2	L	0.2 µm	0.2 µm
	W	2.5 µm	2.5 µm
	M	44	32
M_3	L	0.2 µm	0.2 µm
	W	2.5 µm	2.5 µm
	M	4.4	3.2
L_g	L_g	11.0 nH	4.6 nH
	R_{L_g}	1.1 ohm	0.5 ohm
L_s	L_s	0.59 nH	0.38 nH
	R_{L_s}	0.1 ohm	0.1 ohm
C_{ext}, C_s		0.16 pF	42 fF
L_L		R=60 µm, 2.5 turns	R=60 µm, 2.58 turns
C_L		1.8 pF	/

Table 4.1. Transistor sizes and component values of the 2.5 GHz and 5.25 GHz LNAs.

	2.5GHz	5.25GHz
Noise Figure (NF)	0.62 dB	0.91 dB
Input reflection coefficient (S_{11})	-29 dB	-29 dB
Output reflection coefficient (S_{22})	-15 dB	-15 dB
Voltage gain (S_{21})	19.1 dB	17.7 dB
Reverse isolation (-S_{21})	40 dB	40 dB
Third-order intercept point (IIP3)	-2.6 dBm	-2.8 dBm
Supply voltage	1.8 V	1.8 V
Power consumption	9 mW	9 mW

Table 4.2. Summary of the simulated performance of the 2.5 GHz and 5.25 GHz LNAs.

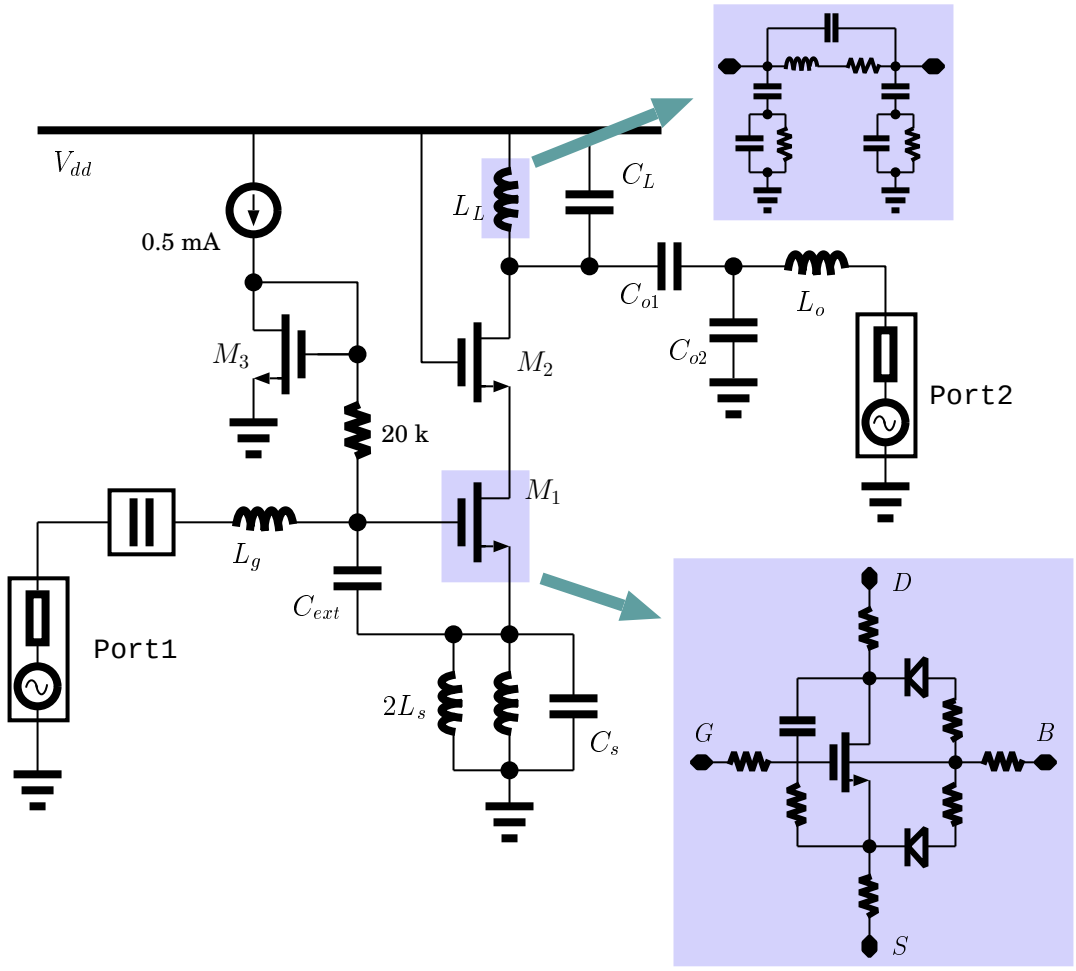


Figure 4.13. LNA schematic for simulations.

is decided by the value of C_{ext} divided by the unit capacitance between metal layers 5 and 6. In the 5.25 GHz LNA design, for a very small value of the C_{ext}, metal layer 5 can be removed and using metal layer 6, 4 to form the extra capacitor for a reasonable bond-pad size. The source capacitance C_s has negligible effect on the noise performance, although is included in the simulations.

4.3 Mixer Design

The second stage in a direct downconversion receiver is the mixer, which performs the required frequency translation. There are two different types of mixers classified as passive mixers and active mixers. A CMOS passive mixer contains four MOSFET switches driven

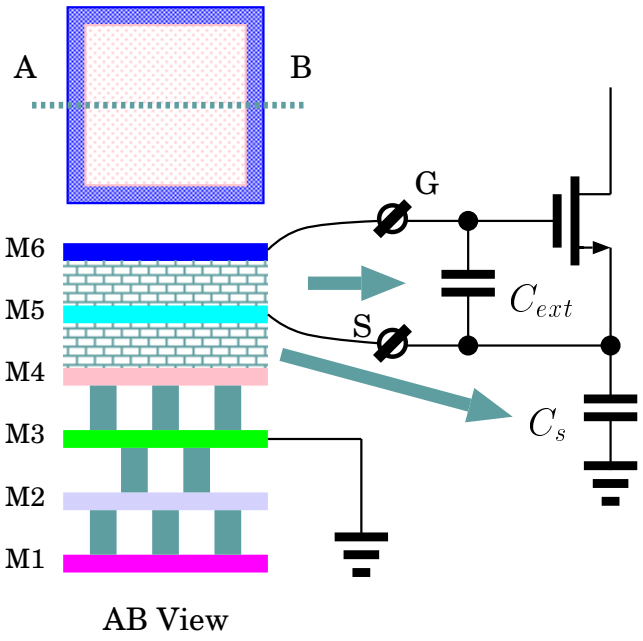


Figure 4.14. Structure of the RF bond-pad provides C_{ext} and ground shield.

by a differential LO signal to convert the frequency as illustrated in Figure 4.15. Since there is no DC bias current in the MOSFET switches, a passive mixer does not consume power, and has no conversion gain. In contrast it has a gain loss. The loss of the conversion gain could be a limitation for a passive mixer, when used in a direct downconversion receiver. Due to the lack of the IF amplifier, the signal is still weak after being translated to the baseband. With the strong impact of the flicker noise at the baseband, the receiver noise figure would be significantly degraded if the mixer has a gain loss.

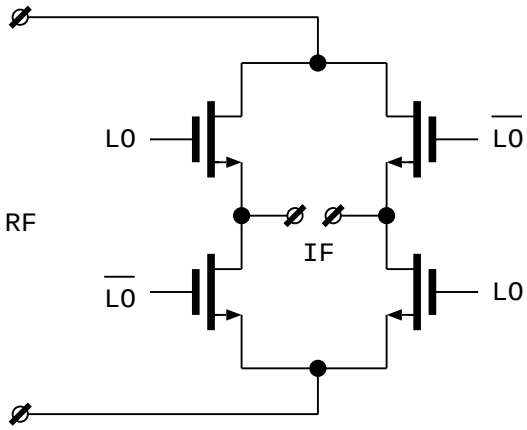


Figure 4.15. Schematic of a CMOS passive mixer.

For the purpose of the conversion gain, active mixers based on the Gilbert cell architecture, are usually employed for the design of direct downconversion receivers. In this section, the Gilbert mixer fundamentals including the conversion gain and the noise analysis are first introduced. Then the design of a 5.25 GHz downconversion mixer is presented.

4.3.1 Conversion Gain of a Gilbert Mixer

A typical single balanced Gilbert cell is shown in Figure 4.16. This circuit topology was initially developed as a precision multiplier, but also widely used as a mixer when the transistors M_2 and M_3 act like switches driven by a strong differential LO signal. The two MOSFET switches commutating the tail current generated by M_1 to achieve the frequency translation. The equivalent behaviour model of the Gilbert cell for the numerical analysis is illustrated in Figure 4.17. The transconductor g_m represents the voltage-to-current conversion of M_1, and the switching transistors are replaced with two ideal switches.

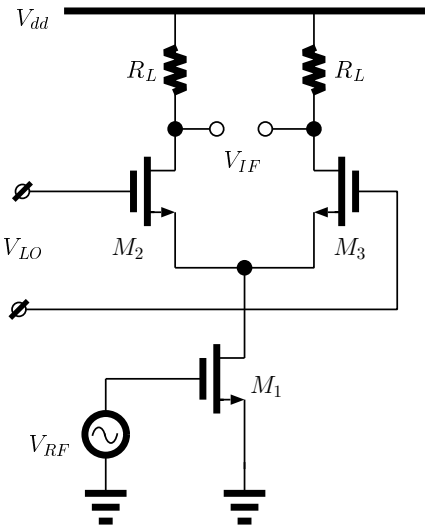


Figure 4.16. Schematic of a single balanced Gilbert mixer.

The differential square-wave LO signal with unity amplitude can be expanded in Fourier series as

$$V_{LO}(t) = \frac{4}{\pi}\left[\cos(\omega_{LO}t) - \frac{1}{3}\cos(3\omega_{LO}t) + \frac{1}{5}\cos(5\omega_{LO}t) - \cdots\right], \tag{4.65}$$

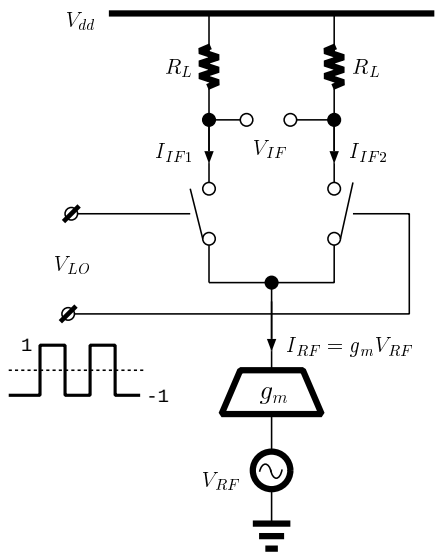


Figure 4.17. Behaviour model of a single balanced Gilbert mixer.

where ω_{LO} is the frequency of the LO square-wave in radians. For a direct downconversion mixer, the fundamental term in Eq. 4.65 translates the RF signal down to the baseband. Assuming the RF input signal is $\cos(\omega_{RF}t)$, thereby the transconductance output current is $g_m \cos(\omega_{RF}t)$, and the downconverted baseband signal is given by

$$\begin{aligned} V_{BB}(t) &= \frac{4}{\pi}\cos(\omega_{LO}t) g_m \cos(\omega_{RF}t) R_L \\ &= \frac{2 g_m R_L}{\pi}\cos[(\omega_{LO} - \omega_{RF})t], \end{aligned} \tag{4.66}$$

where the high frequency term is neglected. Comparing the signal amplitudes at the RF and the baseband gives the voltage conversion gain as

$$A_V = \frac{2 g_m R_L}{\pi}. \tag{4.67}$$

The square-wave LO signal contains odd harmonics, which also downconvert the RF signals at frequencies of $(2n-1)\omega_{LO}$, where $n = 1, 2, 3 \cdot \cdots$. Therefore, high frequency interferers must be sufficiently attenuated by an RF filter before the downconversion, when a square-wave LO signal is applied.

In reality, the conversion gain is less than the value calculated by Eq. 4.67. This is because an ideal square-wave LO signal is unachievable and the switches cannot operate abruptly. Therefore, in every LO period there is a short time that both switches are on, sharing the tail current. Neglecting the MOSFET sub-threshold region of operation, the

overlapped LO signals V_{LO+} and V_{LO-} can be modelled as square waves with unequal high and low periods as depicted in Figure 4.18. The equivalent differential LO signal is equal to $V_{LO+} - V_{LO-}$. Expanding V_{LO+} and V_{LO-} into Fourier series and calculating for the differential LO signal gives

$$\begin{aligned} V_{LO}(t) &= V_{LO+} - V_{LO-} \\ &= \frac{4}{\pi}\cos(2\pi\kappa)\cos(\omega_{LO}t) + O[\cos^3(\omega_{LO}t)], \end{aligned} \tag{4.68}$$

where κT_{LO} in Figure 4.18 represents the period that the two switching transistors are all on. Comparing the fundamental terms of Eqs. 4.65 and 4.68, the non-ideal one is shrunk by a factor of $\cos(2\pi\kappa)$ and the same as the conversion gain. When $\kappa = 0$, the differential LO signal returns to the ideal square-wave, and when $\kappa = 1/4$, the two switches are always on, resulting in zero conversion gain. As a result, the larger LO signal has sharper slope and smaller κ, hence larger conversion gain. However, large LO signal may cause more LO power leaking to the RF port, introducing strong DC offset. In practise, the LO signal power is often chosen between -10 dBm and 0 dBm referred to a 50 ohm load.

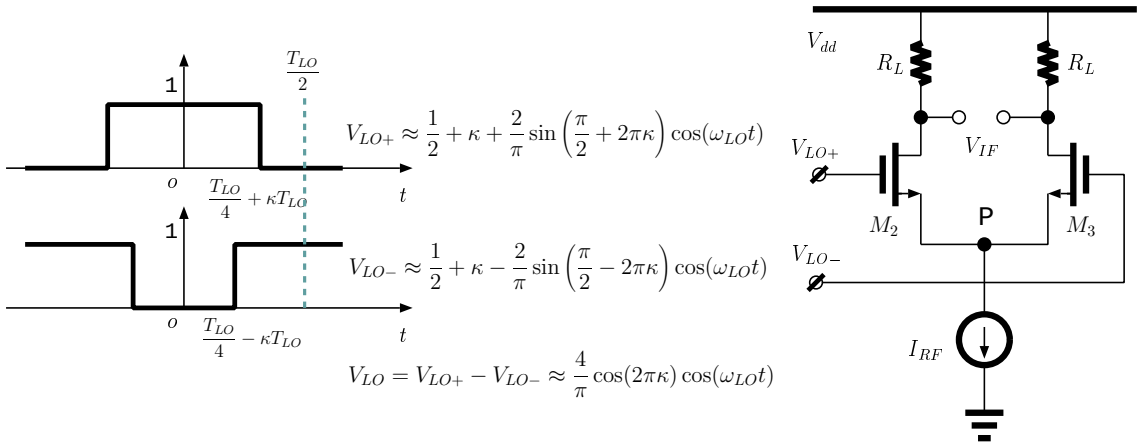


Figure 4.18. Mixer driven by an overlapped differential square-wave LO signal.

In addition to the non-ideal LO signal, the parasitic capacitor C_P at node P causes current leakage, and reduces the conversion gain. As illustrated in Figure 4.19, to reduce the current leakage, an inductor L_D can be put at node P in parallel with C_P to resonate the parasitic capacitor around the RF. This inductor also reduce the flicker noise introduced by M_1 due to its low impedance at low frequencies.

The mixer conversion gain is also related to the LO DC bias $V_{LO_{DC}}$, because the transconductance g_m of M_1 varies with the voltage at node P.

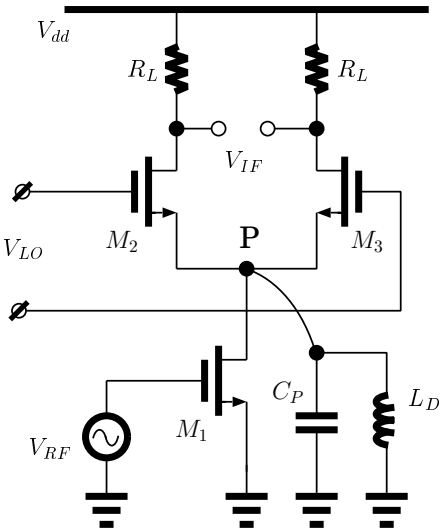


Figure 4.19. Current leakage via C_P is cancelled by inductor L_D.

From the previous discussion, the actual conversion gain of a Gilbert mixer is a function of g_m, V_{LO}, $V_{LO_{DC}}$, C_P and L_D if used. Accurate estimations of the conversion gain must be obtained by careful simulations.

4.3.2 Flicker Noise In a Gilbert Mixer

In a direct downconversion receiver, the mixer noise issue, especially the flicker noise, is critical, when using CMOS processes. It is important to analysis flicker noise sources in a mixer, and develop circuit techniques to minimise the flicker noise intensity presented at the baseband. The noise sources in a Gilbert mixer can be identified as the load noise, the transconductor noise, and the switch noise.

The flicker noise from the loads can be lowered by using poly-silicon resistors or PMOS transistors with large dimensions. Resistors have negligible flicker noise compared to MOS transistors. However the mixer conversion gain requires large current and resistance, thus a large voltage headroom. PMOS transistors present much lower flicker noise than the NMOS counterpart with the same dimensions, and only consume V_{dsat} to remain in the saturation region.

For a low voltage design, the combination of resistors and PMOS transistors [23], sometimes referred to as the current bleeding technique [24], introduces good performance.

As illustrated in Figure 4.20, the PMOS transistor M_4 provides about 70% of the bias current required by M_1 for a large transconductance. Only 30% of the current flow through the load resistors, therefore large resistors can be applied for the better conversion gain.

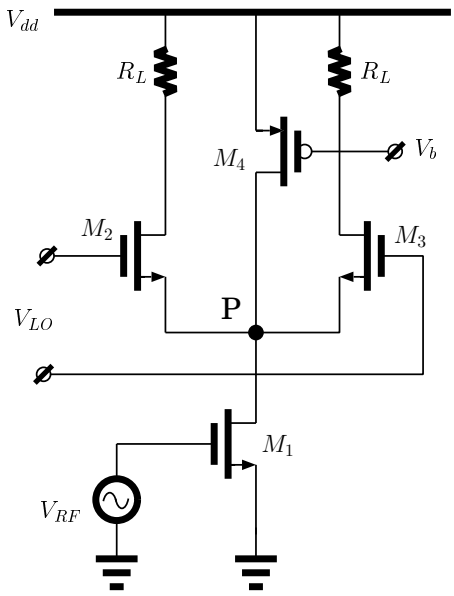


Figure 4.20. Single balanced mixer with the current bleeding technique.

The flicker noise $V_{1/f}$ presented at the mixer input is multiplied by the LO signal expressed in Eq. 4.65, In an ideal mixing process, the power spectrum of $V_{1/f}$ is frequency translated to the LO frequency region. However, in reality, due to the device mismatches between the differential paths, the differential LO signal may exhibit a DC component α, which generates an output term of $\alpha V_{1/f}$ without frequency translation, as depicted in Figure 4.21. This effect is referred to as the "mixer direct feedthrough" [3]. Direct feedthough of the flicker noise and also the second-order harmonic degrades the mixer noise figure at low frequencies. With a proper layout of the differential paths, the mixer direct feedthrough can be minimised in an integrated receiver design.

The last flicker noise source is from the switching transistors. At first glance the flicker noise of the switching transistors is also frequency translated to the LO frequency region, but actually this is not true. In [25], the authors introduced simple but intuitive mixer models to analyse the flicker noise, and concluded a direct and an indirect mechanisms that the flicker noise feeds through the mixer. Similar models in [25] are used here to investigate the flicker noise issue due to the switching transistors and contribute some extra results. Three different processes whereby the flicker noise of the switches appeared

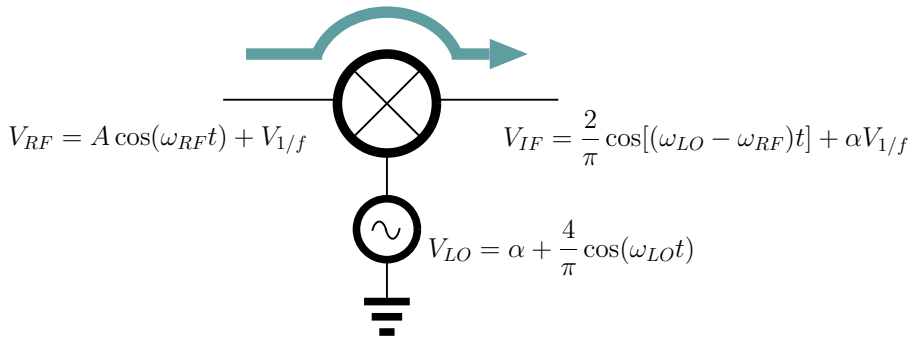


Figure 4.21. Low frequency noise introduced by the mixer direct feedthrough.

at the mixer output are discussed.

A. Self-modulation

As illustrated in Figure 4.22, i_{n2} and i_{n3} are the flicker noise currents of the switching transistors M_2 and M_3 respectively. In order to evaluate the output flicker noise current, the differential LO signal is separated into V_{LO+} and V_{LO-}, and expanded using Fourier series as

$$V_{LO+}(t) = \frac{1}{2} + \frac{2}{\pi}\cos(\omega_{LO}t) + O[\cos^3(\omega_{LO}t)], \quad (4.69)$$

$$V_{LO-}(t) = \frac{1}{2} - \frac{2}{\pi}\cos(\omega_{LO}t) + O[\cos^3(\omega_{LO}t)]. \quad (4.70)$$

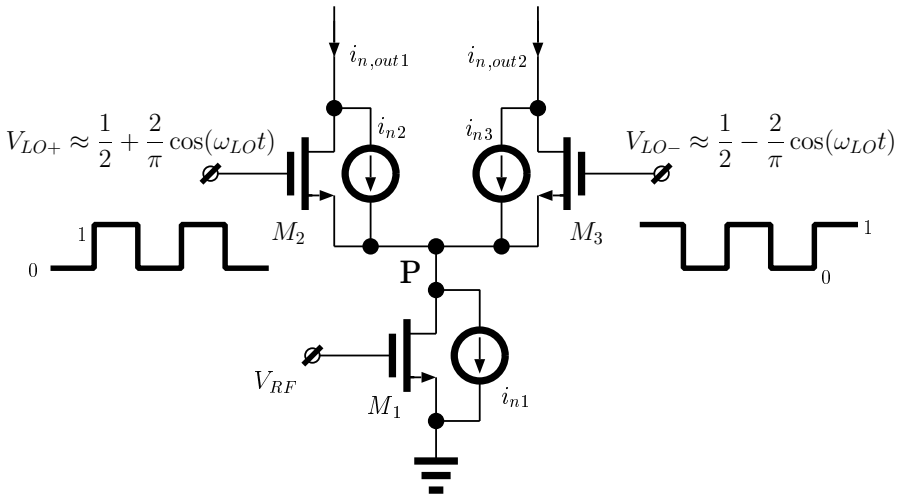


Figure 4.22. Switching transistor flicker noise self-modulation process.

The fundamental terms in Eq. 4.69 and Eq. 4.70 downconvert the RF signal to the baseband yielding a conversion gain given by Eq. 4.67, and also translate the flicker noise power to the LO frequency region. However the DC components allow the flicker noise to feedthrough through the mixer with a gain of 1/2. For the flicker noise current i_{n1} of the transconductor M_1, the feedthrough components of the two differential paths are identical and hence are cancelled when considering the differential output. But the flicker noise of the switches has a different situation. Since V_{LO+} and V_{LO-} modulate their own uncorrelated noise sources i_{n2} and i_{n3}, the two flicker noise current cannot cancel each other at the differential output. The differential flicker noise at the mixer output has a feedthrough component given by

$$i_{n,out} = \frac{1}{2}(i_{n,out1} - i_{n,out2}) \approx \frac{1}{2}(i_{n2} - i_{n3}). \tag{4.71}$$

The self-modulation mechanism shows that the flicker noise feedthrough is inevitable in a Gilbert mixer, even with an ideal LO signal.

B. Indirect Switch Noise

The indirect switch noise process [25] happens when the parasitic capacitor C_P at node P is taken into consideration. As depicted in Figure 4.23(a), during the first half LO period, M_2 is switched on and M_3 is off, so the flicker noise voltage v_{n2} charges C_P. During the second half LO period, M_3 is switched on and M_2 is off, discharging C_P. The same process happens to v_{n3}, resulting in the differential noise model illustrated in Figure 4.23(b).

The time constant of the charge and discharge circuitry is C_P/g_{m2} [25], where g_{m2} is the transconductance of the switching transistor M_2. Assuming that the source follower M_2 has a unity voltage gain, and the time constant is usually much smaller than the LO period, thus the voltage v_P at node P reaches v_n during every charging period, resulting in the average noise current by

$$\begin{aligned} i_{n,out} &= \frac{2}{T_{LO}} \int_0^{T_{LO}/2} C_P \frac{dv_P}{dt} dt \\ &= \frac{2C_P}{T_{LO}} v_n, \end{aligned} \tag{4.72}$$

where T_{LO} is the LO signal period and $v_n = v_{n1} - v_{n2}$ is the differential flicker noise voltage. Eq. 4.72 indicates that the higher LO frequency or the larger parasitic capacitor C_P

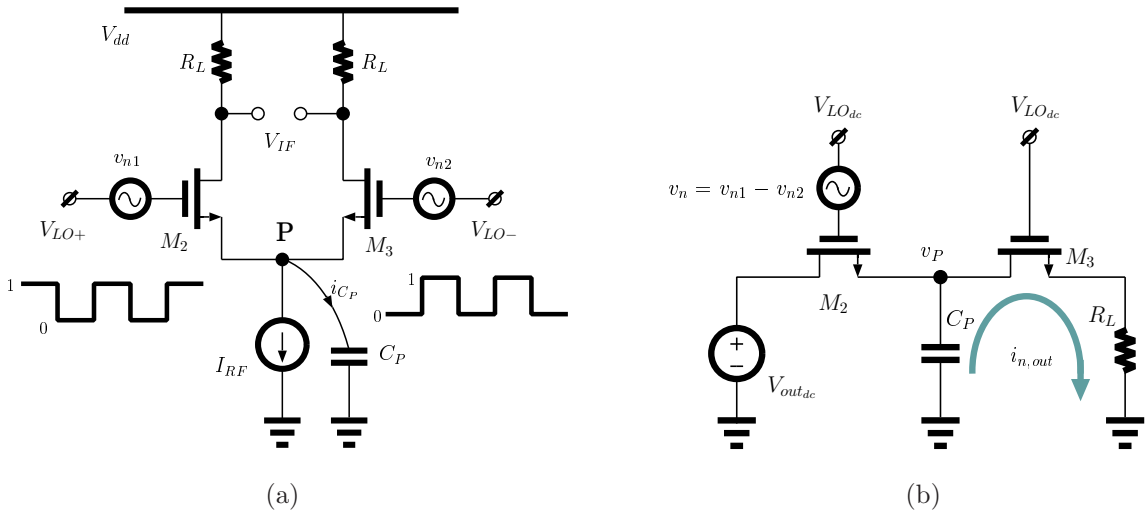


Figure 4.23. (a) Indirect switch noise process due to the parasitic capacitance at node P; (b) differential indirect switch noise model.

results in larger flicker noise at the mixer output due to the indirect switch noise process.

C. LO signal jitter

The LO jitter effect due to the flicker noise at the gates of M_2 and M_3 should be taken into consideration when the LO signals have finite slope during the switching time. Neglecting the MOSFET sub-threshold state and assuming sharply switching, the slowly varying flicker noise associated with the LO signal modulates the time at which M_2 and M_3 switch [25]. As depicted in Figure 4.24, the flicker noise modulation on the LO signal introduces uncertainty of the switching period T_{LO}, similar to the effect of clock jitter. The LO error ϵ, which is a function of the flicker noise v_n and the slope S of the LO signal at the threshold-crossing point, results in the direct switch noise as explained in [25]. Besides the direct switch noise, there is still another process, which allows the flicker noise introduced by M_1 to feedthrough the mixer due to the LO jitter.

The DC terms of the equivalent LO signals with jitter effect are calculated using Fourier series as

$$V_{LO+}|_{DC} = \frac{1}{2} + \epsilon_1(v_{n1}, S), \tag{4.73}$$

$$V_{LO-}|_{DC} = \frac{1}{2} + \epsilon_2(v_{n2}, S), \tag{4.74}$$

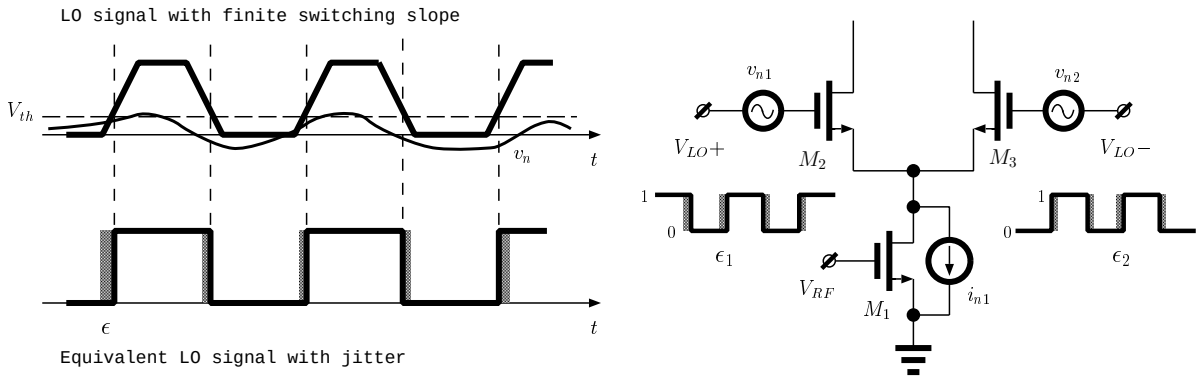


Figure 4.24. Mixer LO signal jitter due to the flicker noise of the switching transistors.

where ϵ_1 and ϵ_2 are uncorrelated LO errors of M_2 and M_3 respectively. Therefore the differential LO signal contains a DC component $\Delta\epsilon = \epsilon_1 - \epsilon_2$, which allows the feedthrough of the flicker noise current of M_1, given by

$$i_{n,out} = i_{n1}\Delta\epsilon. \tag{4.75}$$

According to the previous analysis, several considerations can be taken to improve the mixer noises figure: (1) using resistive loads with current bleeding technique to reduce the flicker noise of the loads and the switching transistors; (2) proper layout design to improve the symmetry of the differential paths; (3) employing an inductor L_D to reduce the low frequency impedance and the parasitic capacitor effect at node P; and (4) using square-wave LO signal, if applicable, to minimise the LO signal error.

4.3.3 Circuit Design of a 5.25 GHz Gilbert Mixer with inductor degeneration

Figure 4.25 illustrates a 5.25 GHz mixer for the direct downconversion receiver. The mixer core is based on a double-balanced Gilbert cell. The tail current source underneath the transconductors M_1 and M_2 is removed to favour the low voltage supply. The linearity of the directly grounded transconductor is also better than that with a tail current source [26].

The current bleeding transistors M_7 and M_8 supply about 70% current for the transconductors. The resistor loads are chosen as 900 ohm that deliver the rest current. Less current flowing through the switching transistors also improves the noise figure

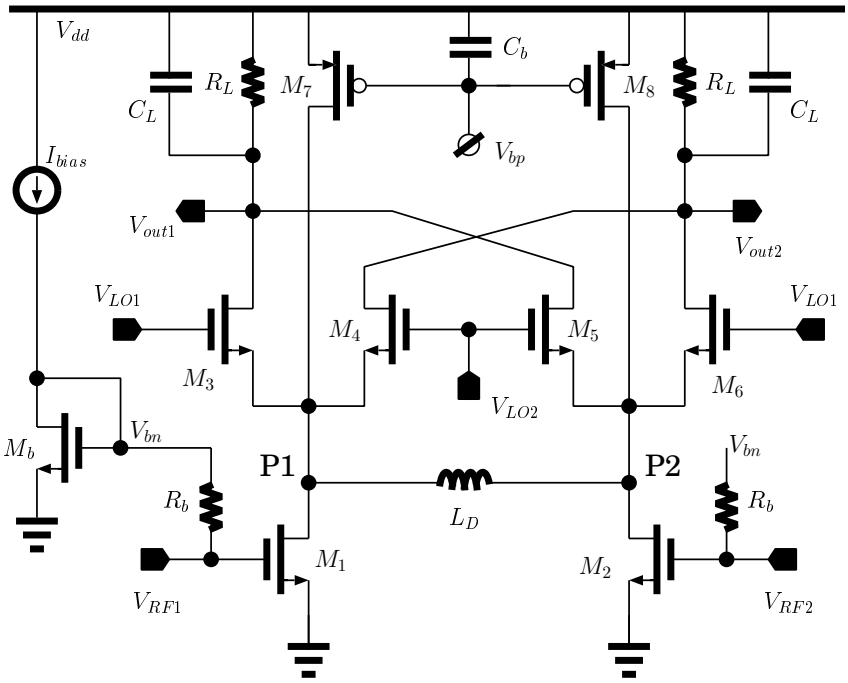


Figure 4.25. Schematic of the 5.25 GHz direct downconversion mixer.

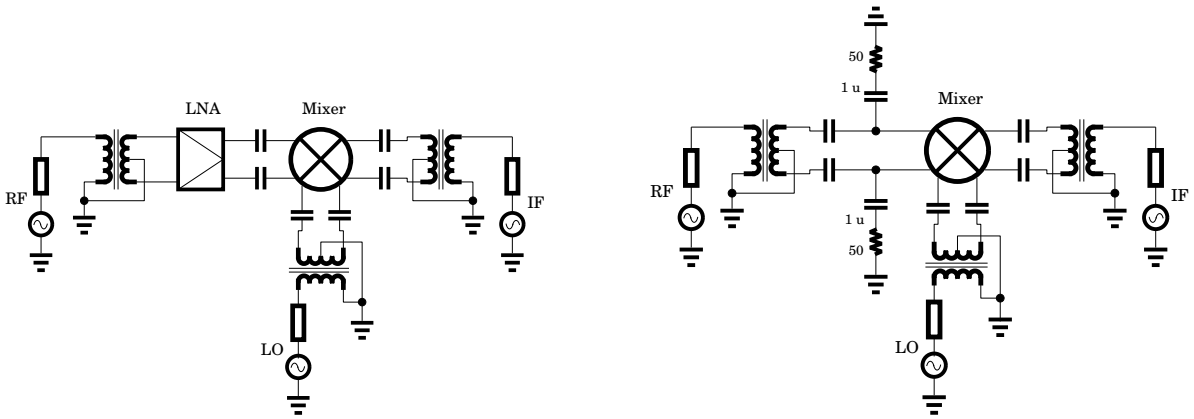
[27]. Two capacitors are in parallel with the resistor loads, facilitating an RC lowpass pole at the baseband edge to relax the linearity criteria of the subsequent baseband circuitry [28].

The switching transistors $M_3 \sim M_6$ are biased near their threshold voltage for the better linearity [26], while keeping the transconductors M_1 and M_2 in the saturation region.

The inductor L_D resonates with the parasitic capacitance presented at nodes P1 and P2 around RF to improve the conversion gain and the low frequency noise figure. However, too large conversion gain reduces the receiver linearity, therefore an optimised inductance value is obtained by simulations as a trade-off between the conversion gain, noise figure and the linearity.

The mixer is designed to drive a high input impedance amplifier, thus is unbuffered. The test LO signal is a differential sinusoid with 0 dBm power referred to 50 ohm loads. The detailed device parameters are listed in Table 4.3, and the simulated performance is presented in Table 4.4. The noise figure was simulated with the combination of the LNA and mixer, as illustrated in Figure 4.26(a), since the mixer input ports are not matched

to 50 ohm. For the conversion gain and linearity simulations, broadband matching using resistors are employed as shown in Figure 4.26(b). The IIP3 was simulated with two input sinusoids at 5.255 GHz and 5.256 GHz respectively.



(a) (b)

Figure 4.26. (a) LNA, mixer combination for the NF simulation; (b) broadband input matching for other mixer simulations.

M_1, M_2	L	0.4 µm	$M3 \sim M6$	L	0.3 µm
	W	2.5 µm		W	2.5 µm
	M	10		M	76
M_7, M_8	L	0.5 µm	M_b	L	0.4 µm
	W	2.5 µm		W	2.5 µm
	M	20		M	1
I_{bias}		0.2 mA	R_b		20 kohm
R_L		900 ohm	C_L		12 pF
L_D		R=60 µm, 2.5 turns			

Table 4.3. Transistor sizes and component values of the 5.25 GHz downconversion mixer.

4.4 Variable Gain Amplifier Design

In a direct downconversion receiver, because of the lack of the channel-selection filter at the IF, strong interferers maybe in the vicinity of the baseband after downconversion,

Noise Figure (with LNA at 312.5 KHz)	6.7 dB
Noise Figure (with LNA at 5 MHz)	5.5 dB
Conversion gain (with 1 Mohm load)	6.8 dB
Third order intercept point (IIP3)	10 dBm
Supply voltage	1.8 V
Power consumption	7.8 mW

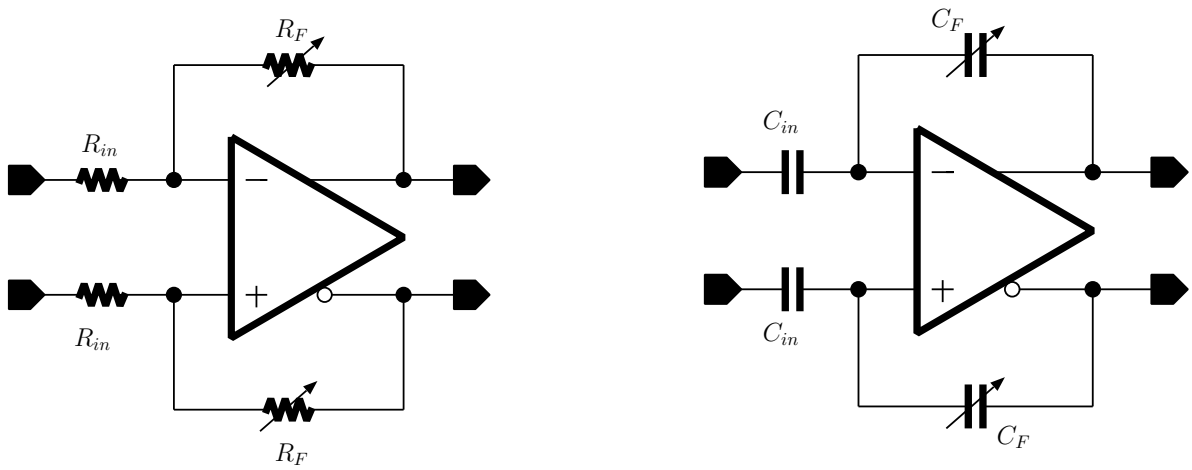
Table 4.4. Simulated performance summary of the 5.25 GHz downconversion mixer.

mandating high linearity in the baseband amplifier. This constraint can be relaxed by using a partial channel-selection lowpass filter before the baseband amplifier [9]. However, a filter before the baseband amplifier degrades the receiver noise performance, because input resistors are usually required for the filter design. For the IEEE802.11a standard as discussed in Chapter 3, the receiver noise figure is crucial, especially at low frequencies when 64-QAM modulation is utilised. Therefore, in this design, a baseband amplifier is used after the downconversion mixer.

The 52 channel OFDM modulation scheme introduces large peak-to-average ratio, hence requires a wide receiver dynamic range. VGAs are often employed in wireless receivers to improve the dynamic range. OTA-R and OTA-C VGA configurations shown in Figure 4.27 provide good linearity. The gain can be adjusted by changing R_F or C_F.

The trade-offs between the two architectures are the noise performance and the silicon area. Input resistors R_{in} in Figure 4.27(a) occupy a small silicon area, but introduce thermal noise before the baseband amplification. The architecture shown in Figure 4.27(b) requires a large silicon area to accommodate the capacitors but provides good noise performance. This is because the input capacitor C_{in} is chosen very large, hence the thermal noise presented on C_{in} is negligible.

An advantage of the OTA-C architecture is that the input capacitor C_{in} can be reused with the highpass filter for the DC offset cancellation, as illustrated in Figure 4.28. The highpass filter corner frequency is chosen as 10 kHz for the negligible effect on the receiver SER as discussed in Chapter 3. The two 10 pF capacitors are built on-chip using MiM structure, and the two 1.6 Mohm resistors are external. An on-chip resistor in the megaohm range is achievable by using a deep triode region MOS transistor [9]. However, the external resistors introduce the best linearity and allows the tuning of the highpass



$$A_v = \frac{R_F}{R_{in}} \qquad A_v = \frac{C_{in}}{C_F}$$

(a) (b)

Figure 4.27. (a) OTA-R and (b) OTA-C VGA architectures.

filter for the test purpose. The feedback capacitors are controlled by a switch array to provide a programmable gain.

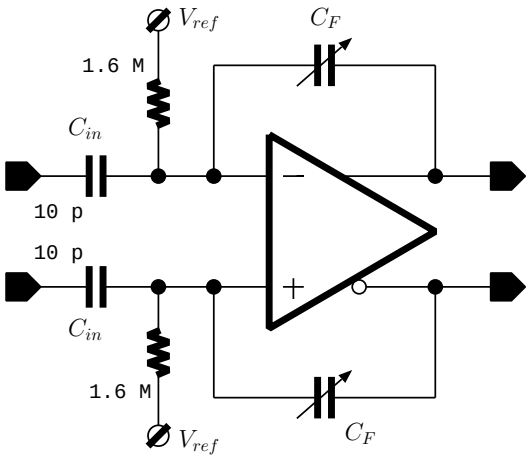


Figure 4.28. OTA-C amplifier and HPF with resused C_{in}.

Single-stage OTAs, such as the telescopic and folded architectures shown in Figure 4.29 are often used for the analog signal processing circuitry design. A telescopic OTA has low power consumption and large gain bandwidth, however requires a higher voltage supply for the stacked MOSFETs load. Whereas a modified low voltage folded

OTA has limited gain and generates more noise because of the two current sources. In this project, a two-stage OTA with a P-type input differential pair due to its low flicker noise is utilised for the VGA. The schematic including the OTA, bias and the CMFB circuitry is shown in Figure 4.30.

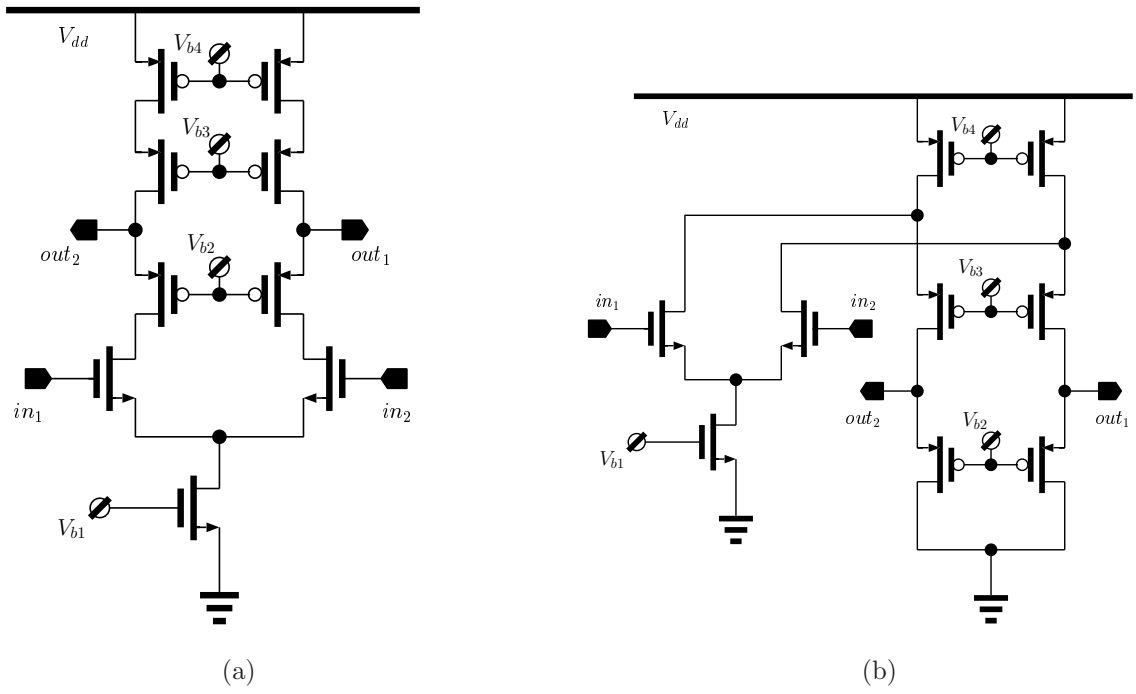


Figure 4.29. Single-stage OTAs. (a) Telescopic; (b) low voltage folded.

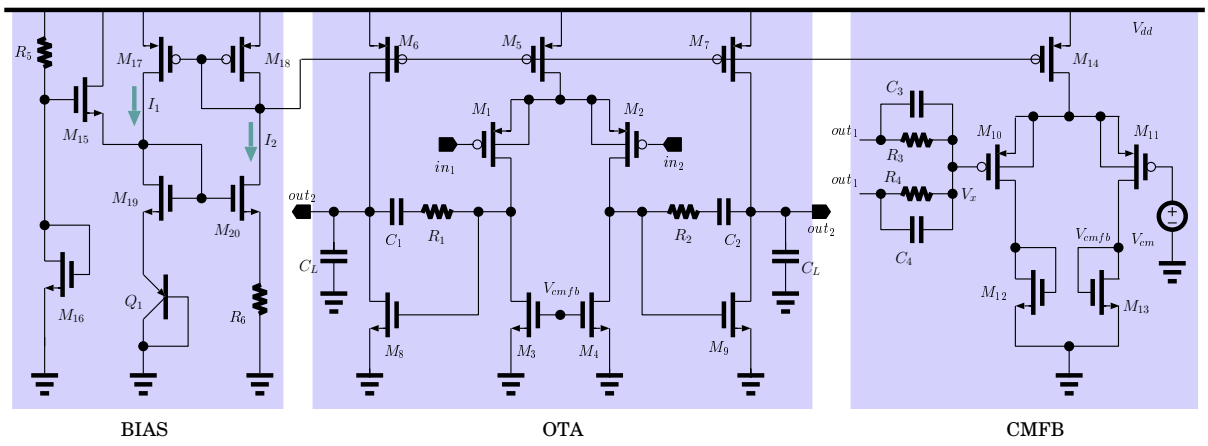


Figure 4.30. Schematic of the two-stage low voltage OTA.

The differential pair M_1, M_2 and M_8, M_9 are the first and second gain stages, biased by M_5 and M_6, M_7 respectively. The total gain can be derived as [29]

$$A_v = \frac{g_{m2}g_{m9}}{I_{ds5}(\lambda_2+\lambda_4)I_{ds6}(\lambda_7+\lambda_9)}, \tag{4.76}$$

where λ_n is the channel length modulation parameter of transistor n. For the frequency response analysis, the OTA half circuit equivalent is shown in Figure 4.31. C_2, R_2 are for the Miller compensation. C_L is the load capacitance at the output nodes. The dominant and the second poles can be approximated as [29]

$$p_1 \approx \frac{-(g_{ds2}+g_{ds4})(g_{ds7}+g_{ds9})}{g_{m9}C_2}, \tag{4.77}$$

$$p_2 \approx \frac{-g_{m9}}{C_L}, \tag{4.78}$$

and an undesired RHP zero at

$$z_1 \approx \frac{1}{C_2(1/g_{m9}-R_2)}, \tag{4.79}$$

which increases both the gain and the phase shift, challenging the OTA stability. The Miller compensation tries to move the dominant pole toward the origin, but far away for the second pole to increase the phase margin. R_2 is called the nulling resistor that is used for an independent control of the RHP zero. The RHP zero can be either moved to infinity or to the LHP and placed on the second pole p_2, resulting in $R_2 = 1/g_{m9}$ or $R_2 = (C_2+C_L)/(g_{m9}C_L)$ respectively.

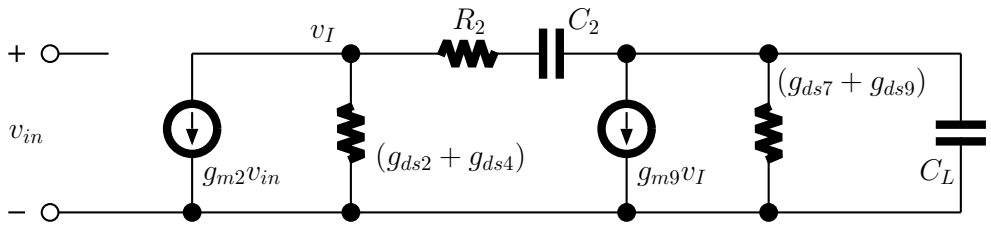


Figure 4.31. Small signal model of the OTA half circuit.

For low noise and large dynamic range purposes, a static CMFB circuit is used. R_3 and R_4 are two large resistors to extract the common mode voltage V_x, which is then compared to the desired DC voltage V_{cm}=0.9 V. V_{cmfb} is then fed back to the OTA current source to force the common mode output pinning at V_{cm}.

In the low voltage bias circuitry, Q_1 generates a supply-independent voltage reference V_{be} and a current reference of

$$I_2 = \frac{V_{be}}{R_6} = \frac{V_T}{R_6} \ln\left(\frac{I_1}{I_s}\right), \tag{4.80}$$

where V_{bs} and I_s are the base-emitter voltage and the junction saturation current of Q_1 respectively. The OTA current biases are setup by mirroring I_2 through M_{18}. A bandgap reference can be used if a temperature-independent current source is desired at the cost of an extra OTA.

R_5, M_{15} and M_{16} are the startup circuit to avoid zero current equilibrium state. M_{15} is turned off when I_1 and I_2 are correctly setup after power on.

Figure 4.32 shows the simulated frequency response of the low voltage OTA. The open-loop DC gain and phase margin are 67 dB and 68 degrees respectively. The unity gain bandwidth is 683 MHz to accommodate the 9 MHz bandwidth for the VGA. The OTA consumes 2 mA current from a 1.8 V voltage supply, including the bias and CMFB circuits.

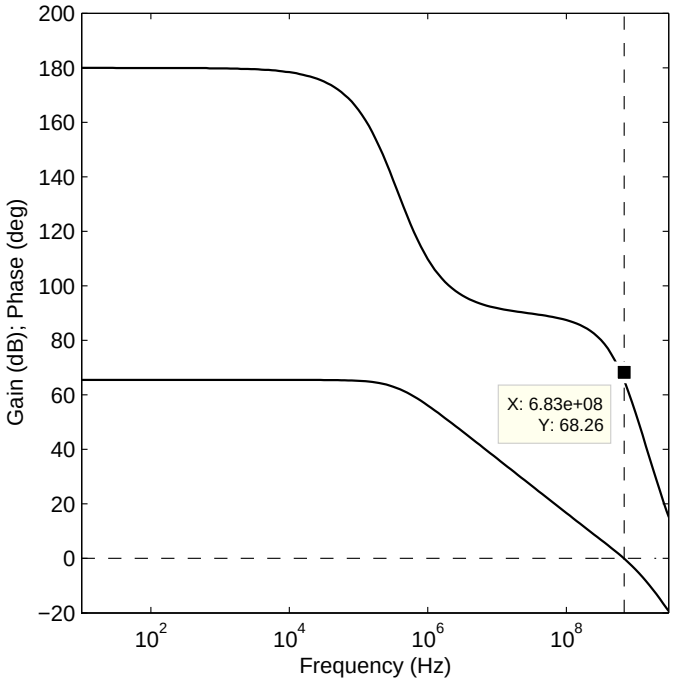


Figure 4.32. Simulated gain and phase responses of the two-stage OTA.

The simulated frequency responses of the highpass filter and VGA combination shown in Figure 4.28 are presented in Figure 4.33 with different gains set by C_F. For the highest

VGA gain configuration, 9 MHz bandwidth is achieved because of the high gain bandwidth of the OTA. As expected, the OTA-C VGA only increases the noise figure by 0.2 dB, when simulated with the receiver frontend circuitry.

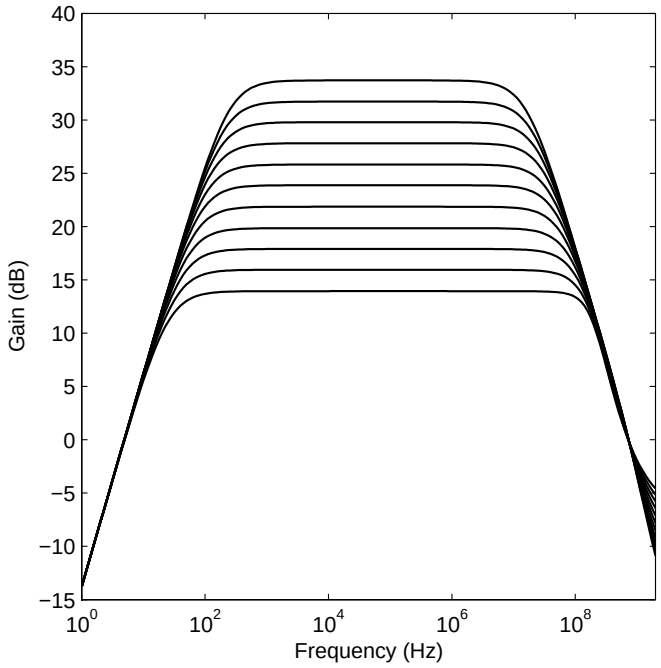


Figure 4.33. Simulated frequency response of the VGA with different gains.

4.5 Channel-selection Filter Design

The design of the channel-selection filter is a trade-off between the channel selectivity, circuit complexity and power dissipation, because every increment of the filter order requires at least one extra OTA. A total sixth-order lowpass filter, which has a 9 MHz corner frequency and 20 dB attenuation at 11 MHz, is chosen as a compromise.

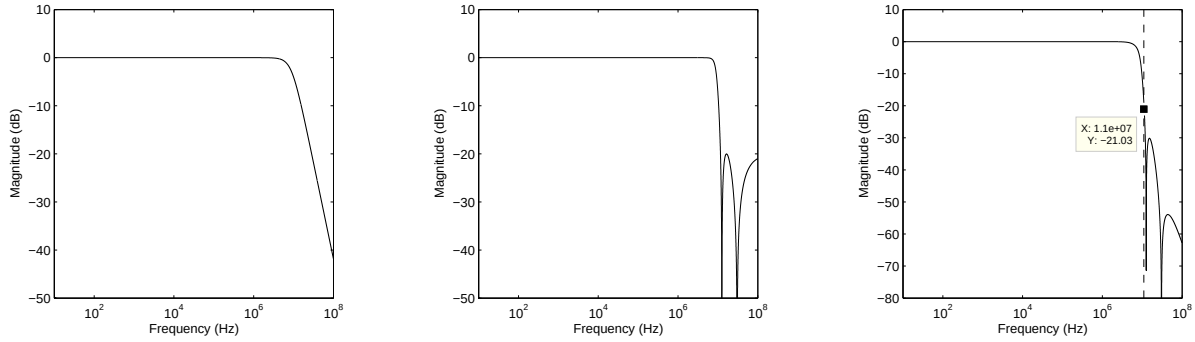
The sixth-order channel-selection filter is separated into two sections. The first part is a second-order Butterworth lowpass filter to suppress the ripples in the stopband, and the second part is a fourth-order Chebyshev II lowpass filter, which has a flat response in the passband and ripples in the stopband. The synthesised transfer functions of the Butterworth and Chebyshev II lowpass filters are

$$H(s) = \frac{3.198e15}{s^2 + 7.997e7s + 3.198e15} \tag{4.81}$$

and

$$H(s) = \frac{0.1e-3s^4 + 4.272e15s^2 + 2.281e31}{s^4 + 1.653e8s^3 + 1.408e16s^2 + 6.69e23s + 2.281e31}. \tag{4.82}$$

The calculated frequency responses of each filter and the combination of the two are shown in Figure 4.34. The total sixth-order channel-selection achieves -20 dB at 11 MHz, as illustrated in Figure 4.34(c).



(a) (b) (c)

Figure 4.34. Calculated frequency responses of (a) the 2nd-order Butterworth LPF, (b) the 4th-order Chebyshev II LPF, and (c) the combination of (a) and (b).

Another VGA/HPF stage is inserted between the two lowpass filters to remove the DC offset and provide sufficient gain. The VGA and the channel-selection filter structures are shown in Figure 4.35. A biquad and a leapfrog topologies are utilised for the Butterworth and Chebyshev II filters implementations. The OTA element for the filters is the same as that for the VGA, but with less current consumption for the PMOS differential pair. As a high gain is not required from the filter and hence the OTA gain bandwidth criteria is much relaxed compared to that in the VGA.

HSPICE simulations of the overall baseband frequency responses, including two VGAs and two lowpass filters, are shown in Figure 4.36. The two VGAs controlled by a six-bit switch array contributes 10∼66 dB gain with 1 dB step for the AGC algorithm, and the total six-order lowpass filter selects the 9 MHz baseband channel.

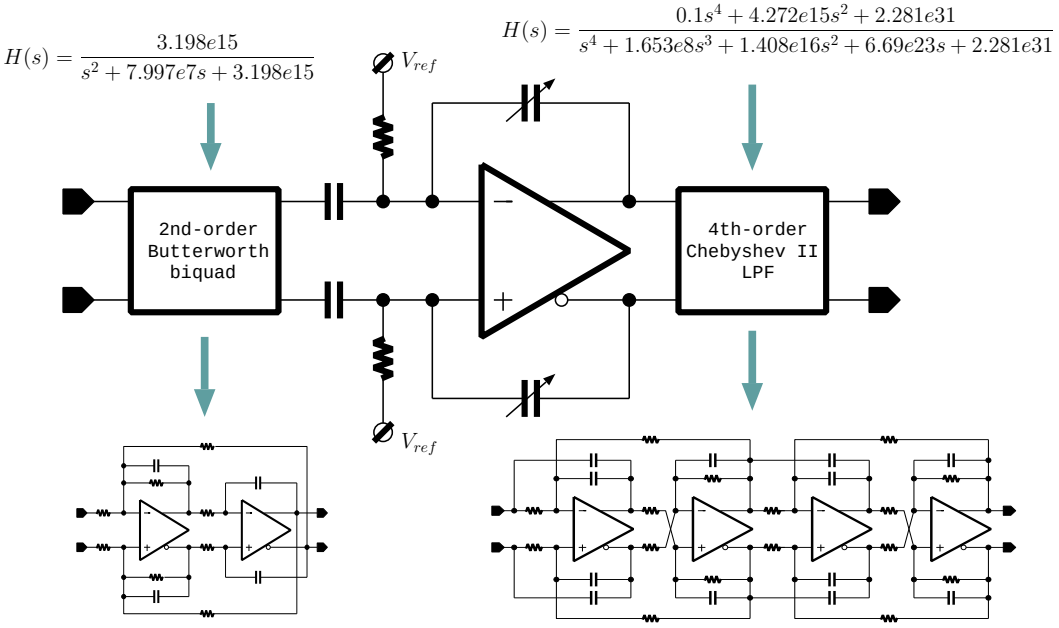


Figure 4.35. Block diagram of the channel-selection filter and the VGA.

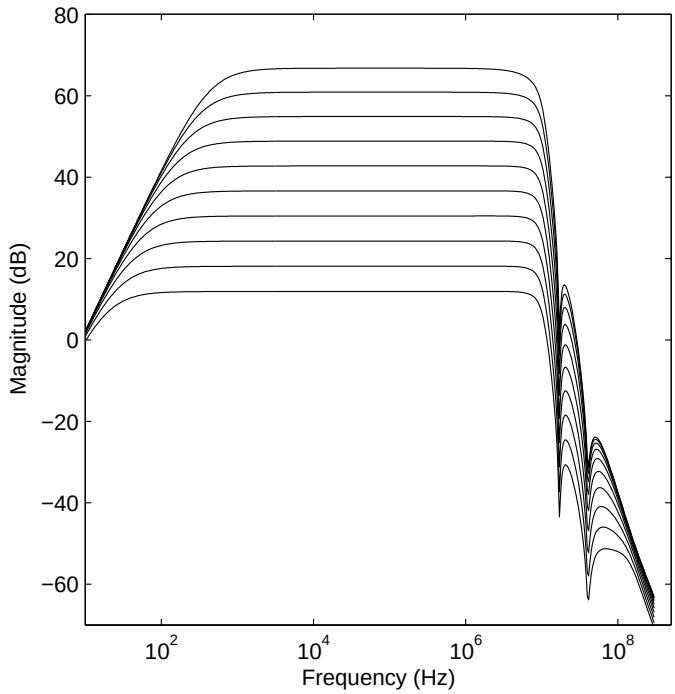


Figure 4.36. Simulated frequency response of the baseband circuit.

4.6 Summary

The design of an IEEE802.11a receiver based on the direct downconversion architecture is presented. The novel (I_{ds}, Q_{in}) LNA design methodology converts part of the gate capacitance to the transistor for a smaller dimension and results in a good noise performance. The mixer physical model analysis reveals that there are multi-mechanisms for the flicker noise to feedthrough the mixer and appears at the baseband. However, with a proper design, the receiver frontend with 8 dB noise figure at 312.5 kHz is achievable using the TSMC 0.18 µm CMOS process.

The VGA based on OTA-C configuration is applied after the mixer as a frontend-to-baseband interface to achieve a better noise performance. Although the OTA-C circuitry occupies large silicon area, it only increase the noise figure by 0.2 dB. The 10 pF capacitors in the VGAs are re-used in the highpass filters for the DC offset removal to improve the silicon area efficiency.

The second-order Butterworth LPF and the fourth-order Chebyshev II LPF select the baseband channel. The total sixth-order lowpass transfer function has ripples only in the stop band, but flat in the passband, so has no effect on the baseband signal. The adjacent interferers are attenuated by 20 dB at 11 MHz by the channel-selection filter.

The overall receiver diagram is illustrated in Figure 4.37. The I, Q channels are identical, but with quadrature LO signals. The receiver performance comparison of published results in [30], [31], [32], [33], and [34] is listed in Table 4.5.

	[30]	[31]	[32]	[33]	[34]	This Work
Technology	0.35 µm SiGe	0.25 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	BiCMOS 35GHz f_T	0.18 µm CMOS
Application	WCDMA	IEEE802.11a	IEEE802.11a	IEEE802.11a	WCDMA	IEEE802.11a
Supply Voltage	1.8 V	2.5 V	1.8 V	1.8 V	2.5 V	1.8 V
Rx Noise Figure	3 dB	8 dB	6.8 dB	5.6 dB	3.1 dB	6.7 dB
IIP3	-14/3 dBm	NA	-25 dBm	-1/-23 dBm	-19.5 dBm	-7.8/-4 dBm
Power consumption	59.4 mW	250 mW	171 mW	212 mW	83 mW	50 mW

Table 4.5. Receiver performance comparison of published results in [30], [31], [32], [33], and [34].

After the downconversion stage, analog-to-digital converters are required for digital phase detector and other DSP algorithms. Sigma-Delta modulation ADCs are chosen, because with today's advanced submicron CMOS process, ultra fast SDM ADCs are achievable to digitise 10 MHz baseband signals by comparatively simply circuitry. The next

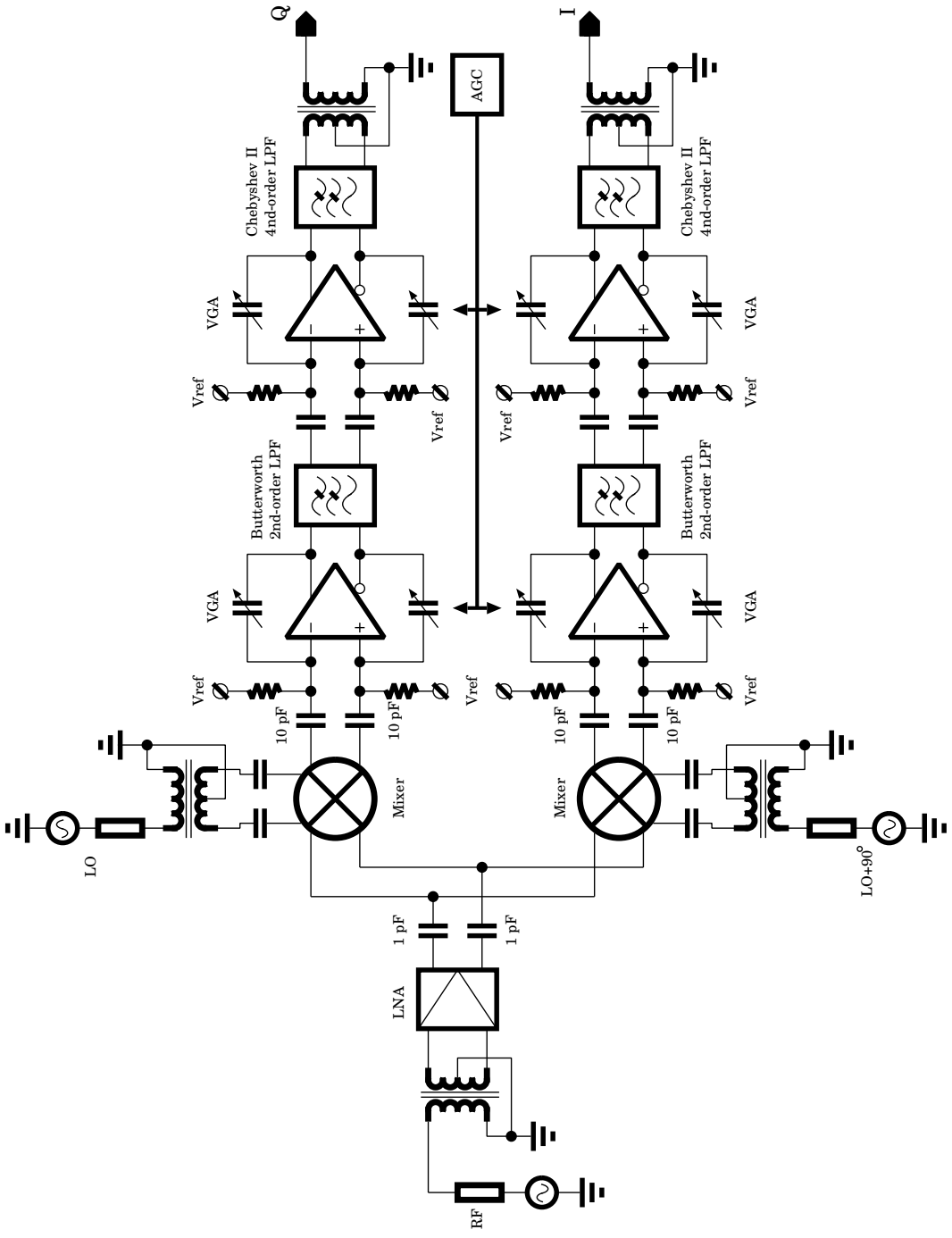


Figure 4.37. Block diagram of the direct downconverstion receiver.

chapter introduces the fundamentals of SDM based on oversampling and noise shaping techniques.

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Chapter 5

Sigma-Delta ADC Fundamentals

5.1 Introduction

As bridges connecting the real world and the digital world, ADCs play important roles in Mixed-Signal systems. As one of the major application areas, today's wireless receivers require high performance ADCs for large bandwidth analog to digital conversion. This challenge results from the use of modern digital modulation techniques, such as spread spectrum or OFDM, which demand bandwidth in the megahertz region. Conventional Nyquist ADCs sample at the minimum sampling frequency to avoid the challenge of high frequency analog circuit design. However, on the other hand, ADCs sampling at the Nyquist frequency require high order analog anti-aliasing filters to attenuate the out-of-band spectrum, hence complicate the overall system design. Moreover, conventional flash ADCs require high precision analog components, which are very difficult to achieve due to the fabrication process fluctuation.

Oversampling flash converters improve the performance by reducing the entire quantisation error floor and eliminate the need for abrupt cutoffs in anti-aliasing filters. However as discussed in section 5.2, the performance improvement by increasing the sampling frequency is not efficient, compared with the penalties of large power consumption and more difficult sample-and-hold circuitry design. They also suffer from mismatch problems due to the process variation.

All of these factors were the drive toward Sigma-Delta modulation ADCs. An SDM consists of a coarse quantiser (can be as simple as single-bit), a DAC in the feedback loop and a loop filter between the input and the quantiser as illustrated in Figure 5.1. The loop filter can be either DT or CT, acting like a highpass filter to the quantisation error, shaping the error power out of the signal band, hence improving the SNR. This feature, defined as the noise shaping, brings good performance by using a comparatively simple circuitry, which is more tolerant to process variations. However, the design of SDMs has its own concerns, such as the loop filter transfer function synthesis and stability of the overall modulator.

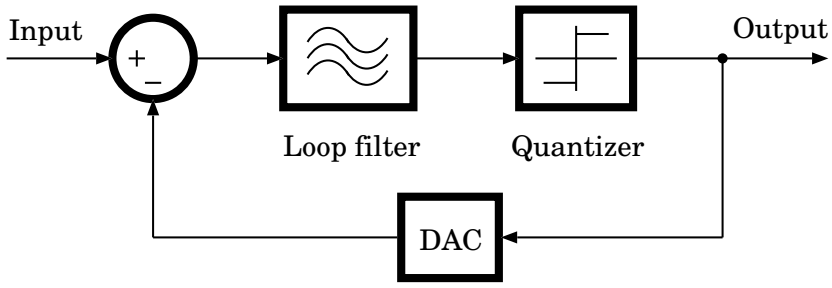


Figure 5.1. Sigma-Delta modulator block diagram

In this chapter, the principles of quantisation error and noise shaping are first introduced in section 5.2 followed by the synthesis methodology of DT NTFs in section 5.3. Next, simulation techniques and spectrum analysis concerns particularly for the SDM design are presented in section 5.4. In section 5.5, the design of BPSDMs by pole-zero rotation is presented. The theory and practise of a DT variable centre frequency BPSDM is introduced in section 5.6. Finally, the design of CT SDMs is discussed in the last section.

5.2 Quantisation Noise and Noise Shaping

All kind of ADCs transfer a continuous analog signal to a finite number of discrete levels represented by a digital code. The difference between the original analog signal and the digital code representation is defined as the quantisation error. As depicted in Figure 5.2, for a 2-bit flash ADC the maximum quantisation error is $\Delta/2$ when the quantiser is not overloaded, where Δ is the quantisation step size. The exact value of the quantisation error can be calculated by the input signal and the quantiser resolution. Therefore the quantisation error is correlated to the input signal, and it is not proper to name it noise.

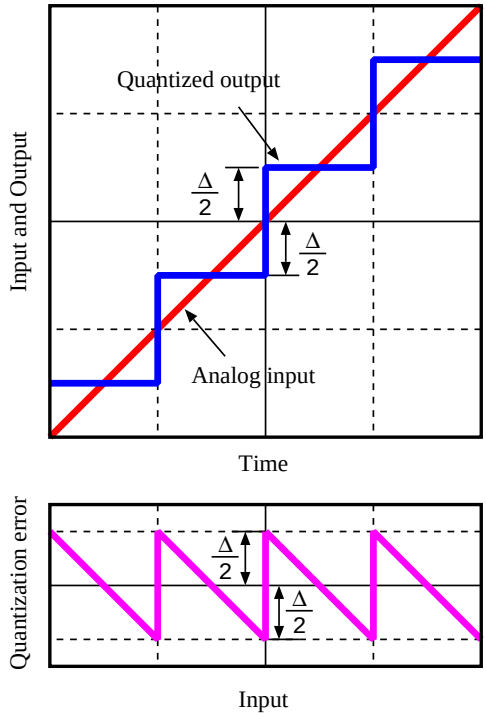


Figure 5.2. Transfer curve and quantisation error of a 2-bit ADC.

5.2.1 White Noise Approximation

One of the most frequently cited paper in ADC area was published in 1948 by Bennett [35]. He first proved that the quantisation error could be modelled as additive white noise if

- the quantiser is not overloaded;
- the bit of the quantiser is large and the step of the quantisation is small;
- the PDF of the quantiser input signal at different sample times is smooth.

When those conditions are met, the PDF of the quantisation error can be derived as

$$p(e_q) \approx \begin{cases} \frac{1}{\Delta}, & e_q \in (-\Delta/2, \Delta/2) \\ 0, & \text{otherwise} \end{cases} \tag{5.1}$$

where e_q is the error sequence and Δ is the quantisation step. The mean value of e_q is given by

$$\overline{e_q} = E\{e_q\} = \int_{-\infty}^{\infty} e_q p(e_q) de_q = \int_{-\Delta/2}^{\Delta/2} e_q \frac{1}{\Delta} de_q = 0, \tag{5.2}$$

and then the mean square power is calculated as

$$\sigma^2{}_{e_q} = E\left\{(e_q - \overline{e_q})^2\right\} = \int_{-\infty}^{\infty}(e_q - 0)^2 p(e_q)de_q = \frac{\Delta^2}{12}. \tag{5.3}$$

In a single-bit SDM, the direct application of Bennett's white noise approximation is not proper, because the conditions are not rigorously met. Nevertheless, extensive early work by Candy [36][37][38] and Gray [39][40], focused on the spectrum structure of a first-order and a second-order SDM, shows that the assumption of the white additive quantisation noise is also approximately valid in SDM systems, and is used in all the modulator transfer function analysis in the literature. The "quantisation error" is often referred to as "quantisation noise", when the white additive noise approximation is applied.

5.2.2 SNR and Oversampling

In a Nyquist sampling ADC, when the white noise approximation is applied to the quantisation error, the mean square noise power is given by $\Delta^2/12$. This noise power is uniformly distributed in the frequency range of $[-f_s/2, f_s/2]$, where $f_s = 2f_B$ is the Nyquist sampling frequency and f_B is the bandwidth. Therefore the noise power inside the baseband is the mean square noise power as shown in Figure 5.3(a).

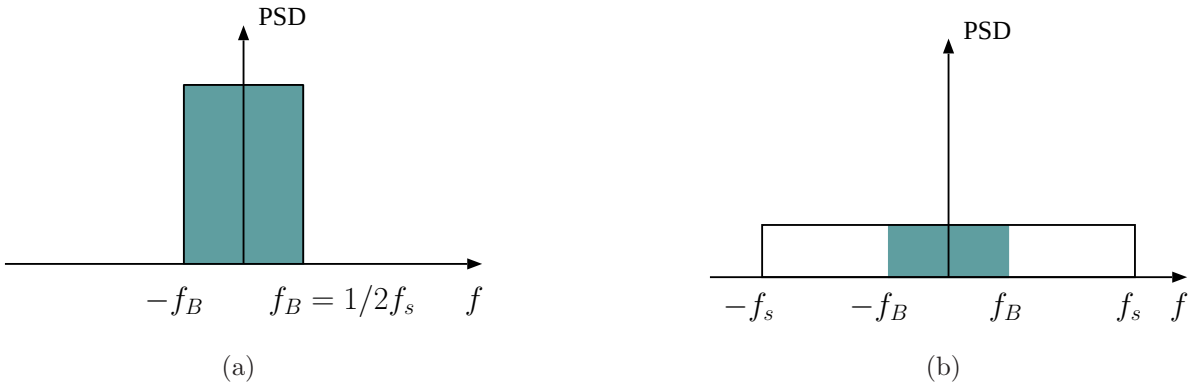


Figure 5.3. Inband noise power inband. (a) Nyquist sampling; (b) oversampling.

The inband noise power can be reduced by increasing the sampling frequency, resulting in an oversampling ADC. The PSD of the oversampled noise power is give by

$$S_{ee}(f) = \frac{\sigma^2_{e_q}}{f_s} = \frac{\Delta^2}{12f_s}. \tag{5.4}$$

The inband noise mean square power, defined as the integral of the PSD over the baseband, is given by

$$\sigma_B^2 = \int_{-f_B}^{f_B} S_{ee}(f)df = \frac{\Delta^2}{12}\left(\frac{2f_B}{f_s}\right). \tag{5.5}$$

Defining the OSR as the sampling frequency f_s divided by the Nyquist frequency $2f_B$, the inband mean square power becomes

$$\sigma_B^2 = \frac{\Delta^2}{12}\frac{1}{OSR} = \frac{\sigma_{e_q}^2}{OSR}. \tag{5.6}$$

As shown in Eq. 5.6, the inband noise power of an oversampling ADC is inversely proportional to the OSR, hence the larger OSR the better resolution. The SNR of an oversampling ADC is given by

$$SNR(\text{dB}) = 10\log\left(\frac{\sigma_s^2}{\sigma_B^2}\right), \tag{5.7}$$

where σ_s^2 is the signal mean square power. The SNR can be written in terms of OSR by substituting Eq. 5.6 into Eq. 5.7, yielding

$$SNR(\text{dB}) = 10\log\left(\sigma_s^2\right) - 10\log\left(\sigma_{e_q}^2\right) + 10\log(OSR). \tag{5.8}$$

Eq. 5.8 shows that every doubling in the OSR increases the SNR by 3 dB only. At the cost of increased power dissipation and much more difficult circuit design to double the OSR, a 3 dB SNR improvement is not a good trade-off.

The quantisation noise power spectrum in a conventional ADC is white, however this is not necessary. If there is an ADC that from the view point of the signal acts as an all pass filter, whereas from the view point of the quantisation noise acts as a highpass filter, which moves the noise power out of the band of interest, then its SNR can be dramatically improved. This concept leads to the noise shaping technique, which is fundamental to SDM ADCs.

5.2.3 Noise Shaping and Sigma-Delta Modulation

As shown in Figure 5.1, in a noise shaping ADC, the highly non-linear quantiser is inside the feedback loop, therefore an SDM is no longer considered as an LTI system. This issue makes it difficult to analyse the noise shaping behaviour using well developed signal processing and control theorems. However, based on the quantiser white noise approximation, the highly non-linear quantiser can be interpreted as a linear summation of the

signal and the quantisation noise, so that the signal processing and the control techniques for LTI systems can be applied. The SDM ADC architecture with the linear quantiser model is shown in Figure 5.4.

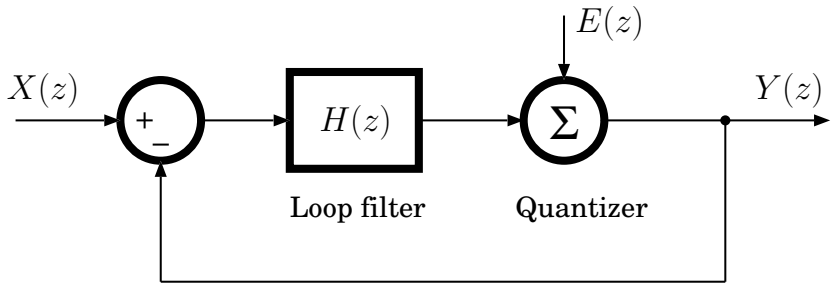


Figure 5.4. Sigma-Delta modulator block diagram with the quantiser linear model.

Assuming the input signal and the loop filter are all discrete, the output of the quantiser $Y(z)$ can be derived in the z-domain as

$$\begin{aligned} Y(z) &= \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}E(z) \\ &= STF(z)X(z) + NTF(z)E(z), \end{aligned} \tag{5.9}$$

where $X(z)$ is the input signal, $H(z)$ is the transfer function of the loop filter, $E(z)$ is the quantisation noise, and

$$STF(z) = \frac{H(z)}{1+H(z)}, \tag{5.10}$$

$$NTF(z) = \frac{1}{1+H(z)}. \tag{5.11}$$

STF and NTF can be thought of as virtual filters working on the input signal and the quantisation noise respectively. For the STF, an all pass filter without distortions on the signal is expected, whereas for the NTF, a highpass filter is desired to shape the quantisation noise power towards the high frequency area. As the simplest case, a first-order NTF can be expressed as

$$NTF(z) = 1 - z^{-1}. \tag{5.12}$$

This results in the STF and the loop filter transfer function as

$$STF(z) = z^{-1}, \tag{5.13}$$

$$H(z) = \frac{1}{z-1}. \tag{5.14}$$

According to Eq. 5.13 and Eq. 5.12, the STF only introduces a unit delay on the signal, whereas the NTF highpass filters the quantisation noise power. The NTF magnitude response can be evaluated by substituting $z = exp(-j2\pi f)$ into Eq. 5.12. The architecture of the first order noise shaping ADC is shown in Figure 5.5. Because of the substractor and the accumulator, this kind of noise shaping ADC is named Sigma-Delta modulator.

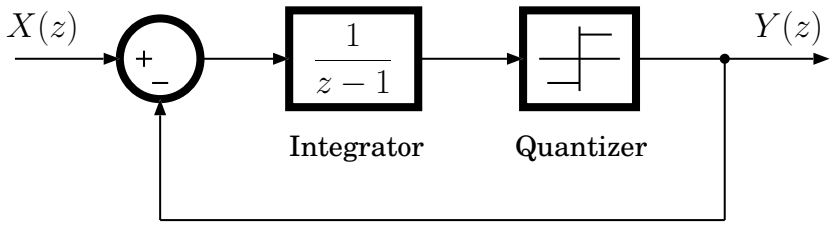


Figure 5.5. First-order SDM block diagram.

The shaped PSD of the quantisation noise power at the SDM output is given by

$$\begin{aligned} S_{ee}(f) &= \sigma_{e_p}^2 \left|1 - e^{(-j2\pi f/f_s)}\right|^2 \\ &= \frac{\Delta^2}{12}\, 4\sin^2\left(\pi \frac{f}{f_s}\right), \end{aligned} \tag{5.15}$$

and the inband noise power is calculated as

$$\begin{aligned} \sigma_B^2 &= \int_{-f_B}^{f_B} \frac{\Delta^2}{12 f_s}\, 4\sin^2\left(\pi \frac{f}{f_s}\right) df \\ &= \frac{f_B \Delta^2}{3 f_s} - \frac{\Delta^2 \sin\left(2\pi \frac{f_B}{f_s}\right)}{6\pi} \\ &\approx \frac{\pi^2 \Delta^2}{36} \frac{1}{OSR^3}, \end{aligned} \tag{5.16}$$

where $\sin(x) \approx x - x^3/6 + o[x]$ is used for the last approximation in Eq. 5.16. Making use of Eqs. 5.7 and 5.16, the SNR can be written as

$$SNR(\text{dB}) = 10\log(\sigma_s^2) - 10\log(\sigma_{e_p}^2) - 10\log\left(\frac{\pi^2}{3}\right) + 30\log(OSR). \tag{5.17}$$

As a result, for the first order SDM, every doubling of OSR increases the SNR by 9 dB, which is 3 times better than the non-shaping oversampling ADC.

To further improve the performance, a high order NTF of $(1 - z^{-1})^M$ can be employed for more efficient noise shaping, where M is the order of the SDM. The magnitude responses of the NTF with different M are illustrated in Figure 5.6. The plot shows that the larger the value of M the better noise shaping.

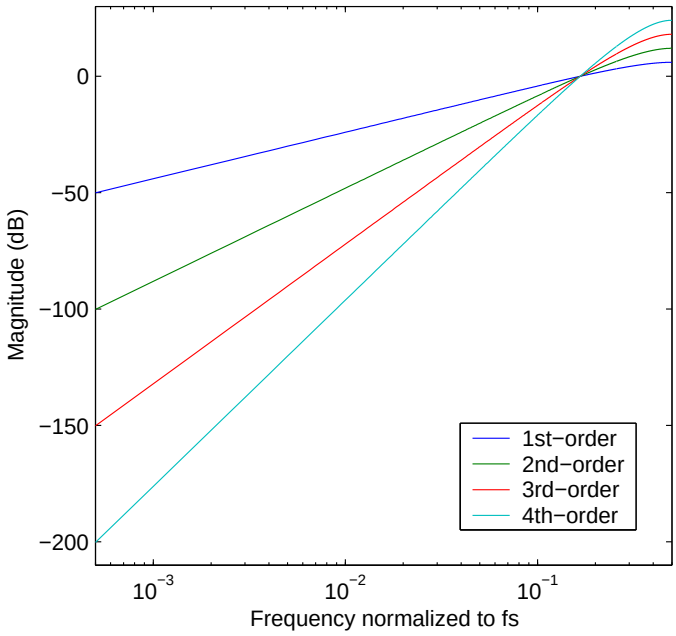


Figure 5.6. Magnitude response of the NTF with different orders.

Following the same procedure, the inband noise power for an M-order SDM can be derived as

$$SNR(\text{dB}) = 10\log(\sigma_s^2) - 10\log(\sigma_{e_p}^2) - 10\log\left(\frac{\pi^{2M}}{2M+1}\right) + (20M+10)\log(OSR). \quad (5.18)$$

Thus, every doubling the OSR improves the SNR by $(6M+3)$ dB and delay the signal by M sampling units.

However this level of performance is not achievable in practise because of the modulator stability issue. In a high order modulator, the signal at the quantiser input may exhibit unbounded state, generally producing a very low frequency oscillation at the output with very poor SNR. This is because all the previous analysis is based on the linear model of the quantiser, which actually is not accurate. The stability criteria of an LTI system does not cover the SDM. Although lots of efforts have been put on the SDM stability issue [41][42][43], the development of a rigorous analysis of the stability criteria has its principle difficulties. There is still lack of an accurate model for the non-linear quantiser located inside the feedback loop. In [44], the authors used simulations and empirical methods to evaluate the high-order SDM stability criteria by controlling the OOBG, and provided a very simple but effective rule-of-thumb to synthesise a stable NTF. Nevertheless, long time simulations of the synthesised modulator are still necessary to evaluate the stability, since none of the SDM stability rules are actually adequate [42].

5.3 Discrete-Time NTF Synthesis

A high order SDM achieves very good SNR because of the efficient noise shaping; on the other hand, stability of the modulators is difficult to achieve. The stability issue makes the SDM design focused on the synthesis of a stable high order NTF. Lee's rule-of-thumb [44], which states that the NTF OOBG should be less than 2, is used as the stability criteria for the NTF synthesis. This rule can be numerically expressed as

$$|NTF(z)|_{z=0.5} \leq 2, \tag{5.19}$$

when the frequency is normalised to the sampling frequency. In addition to the control of OOBG, Lee's rule also suggests a monotonically changing NTF in the passband for the better tolerance to the process variation and maintaining stability of the modulators.

Another constraint on the NTF synthesis is the causality. The NTF can be presented as the ratio of two polynomials as functions of z as

$$NTF(z) = \frac{a_0 + \sum_{i=1}^{M} a_i z^{-i}}{b_0 + \sum_{i=1}^{M} b_i z^{-i}}, \tag{5.20}$$

where a_i, b_i are the numerator and denominator coefficients respectively, and M is the order. Eq. 5.11 can be re-arranged as function of NTF as

$$H(z) = \frac{1 - NTF(z)}{NTF(z)}. \tag{5.21}$$

Substituting Eq. 5.20 into Eq. 5.21, the loop filter $H(z)$ can be written as

$$H(z) = \frac{(b_0 - a_0)z^M + \sum_{i=1}^{M} z^{M-i}}{a_0 z^M + \sum_{i=1}^{M} a_i z^{M-i}}. \tag{5.22}$$

The causality constraint requires at least one unit delay along the loop. This means that the order of the numerator must be smaller than that of the denominator in the loop filter $H(z)$, resulting in $a_0 = b_0$ to eliminate the highest order term of the numerator. Substituting this condition into Eq. 5.20 yields the causality criteria as

$$\lim_{z \to \infty} NTF(z) = 1. \tag{5.23}$$

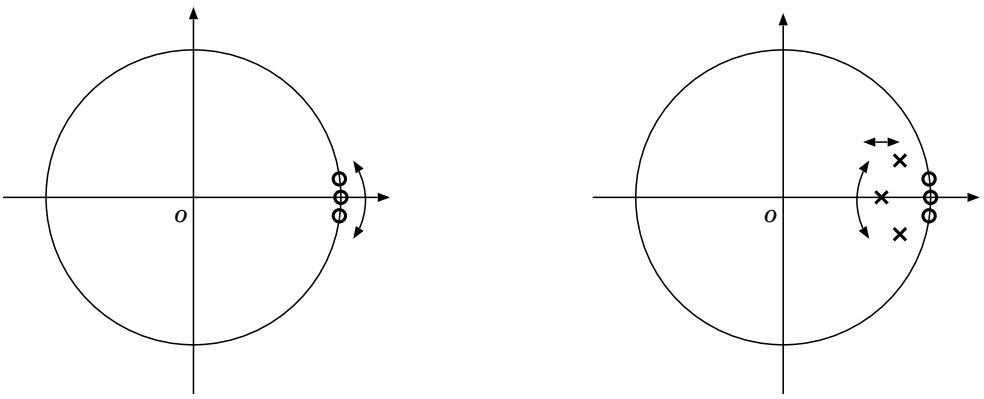
The classic filter design methodology fails to synthesise NTFs. This is because, firstly, classic filters are LTI systems, which have the stability criteria by controlling the poles on

either the s-plane or the z-plane. So the control of the OOBG is not a design constraint for the filter design. Secondly, unlike SDMs, there are no feedback loops enclosing the filters, so that causality is not a constraint for the filter transfer function synthesis. A filter transfer function in 'ZPK' (Zeros, Poles and Gain) mode can be written as

$$F(z) = k\frac{\prod_{i=1}^{M}(z - z_i)}{\prod_{i=1}^{M}(z - p_i)}, \tag{5.24}$$

where z_i are the zeros, p_i are the poles, and k is the gain. When $z \to \infty$, $F(z)$ is equal to k, which normally is less than 1 to have a unity DC magnitude response. Therefore the causality criteria is not met.

A feasible strategy, which has been used in [45], is to separate the synthesis of the NTF zeros and the poles. Firstly, the inband noise power is minimised by adjusting the NTF zeros, and secondly the OOBG is controlled to be less than 2 by tuning the NTF poles, as depicted in Figure 5.7.



Step1: Tune the zeros to minimize the inband noise power.

Step2: Tune the poles to control the OOBG to be less than 2.

Figure 5.7. Separated NTF zeros and poles synthesis.

All the NTF zeros can be put together at DC, called Butterworth type zeros, to form a deep notch at low frequencies. Then the remaining synthesis step is to tune the poles to control the OOBG only. This method is efficient when the bandwidth is very narrow compared to the sampling frequency, or in another term, very large OSR. But for large bandwidth or small OSR applications, Butterworth type zeros are not optimised for the minimum inband noise power. Although the notch is very deep at the DC, the NTF magnitude raises quickly when increasing the frequency, making more inband noise power. As depicted in Figure 5.8, for large bandwidth, split zeros are desired to flatten

the noise PSD inside the signal band. The notch of the NTF magnitude profile at DC is not as deep as that using the Butterworth type zeros, however the target is to gain the minimum noise power inside the broad signal band. Neglecting the NTF poles, the inband mean square noise power can be evaluated by

$$\sigma_B^2(z_1, z_2, \cdots, z_M) = \sigma_{e_q}^2 \int_{-f_B}^{f_B} |(z - z_1)(z - z_2) \cdots (z - z_M)|^2_{z=exp(2j\pi f)} df, \tag{5.25}$$

where $\sigma_{e_q}^2$ is the quantisation noise mean square power expressed in Eq. 5.3, $[z_1, z_2, \cdots, z_M]$ are the NTF zeros located on the unit circle within $(-2\pi f_B, 2\pi f_B)$, M is the order, and $f_B = 1/(2OSR)$ is the bandwidth normalised to the sampling frequency. The searching of the optimised zeros is guided by monitoring Eq. 5.25 for the minimum inband noise power σ_B^2.

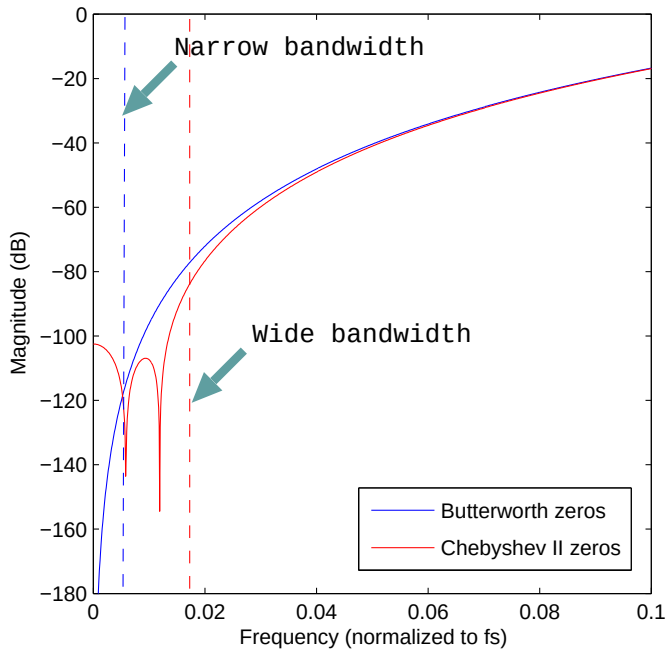


Figure 5.8. NTF magnitude responses with Butterworth and split zeros.

In order to have real coefficients for the filter transfer function, the zeros and the poles of the NTF must be either real values or conjugated pairs, as shown in Figure 5.7. The conjugated zero pairs can be freely moving on the unit circle between $-2\pi f_B$ and $2\pi f_B$. In every searching step, the integral of Eq. 5.25 is calculated. For the synthesis of an M-order NTF, assuming the total searching steps are L, the quantity of the integral calculation is equal to

$$C_L^{floor(M/2)} = \frac{L!}{floor(M/2)![L - floor(M/2)]!}, \tag{5.26}$$

where *floor* is a MATLAB function to find the nearest integer towards $-\infty$. As an example, if $M = 8$ and $L = 1000$, the total integral calculation is 4.14e10. Such a huge integral calculation quantity requires very long time and large computer resources.

To alleviate challenge of the calculation quantity, the NTF zeros should be related to each other to reduce the tuning degrees of freedom. Chebyshev type II zeros are good candidates because they are spread, introducing ripples in the stop band. For an M-order lowpass filter and assuming the corner frequency is 1 rad, Chebyshev type II zeros are located on the imaginary axis of the s-plane at $j/\cos[(2k+1)\pi/2M]$ [46], where $k = 0, 1, \cdots, M-1$. Applying the lowpass-to-highpass transform $s \rightarrow 1/s$ [46], the Chebyshev type II zeros of a highpass filter are located at

$$s_k = j\cos\left[\frac{(2k+1)\pi}{2M}\right]. \qquad (k = 0, 1, \cdots, M-1) \tag{5.27}$$

As illustrated in Figure 5.9, the zeros on the z-plane can be obtained by the bilinear transform, which maps the imaginary axis on the s-plane to the unit circle on the z-plane by

$$\omega = 2\arctan(\Omega), \tag{5.28}$$

where Ω is the s-domain frequency and ω is the z-domain frequency in radians. All the Chebyshev type II zeros are then tuned inside the signal band to find the minimum inband noise power in the z-domain. The flowchart developed for the NTF zeros synthesis is illustrated in Figure 5.10. Since all the zeros follow Eq. 5.27, the searching degree of freedom is only the frequency search steps L. Then, the integral calculation quantity is equal to L.

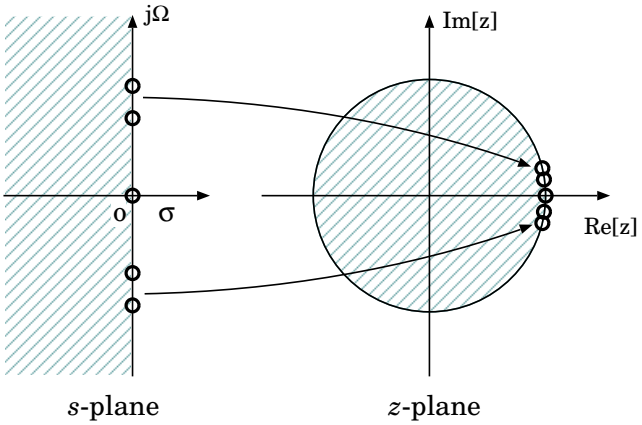


Figure 5.9. Bilinear mapping of the Chebyshev type II zeros from the s-plane to the z-plane.

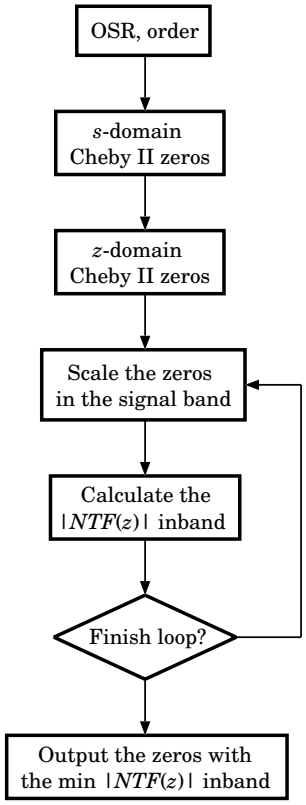


Figure 5.10. Flowchart of the Chebyshev II type zeros synthesis.

When optimised zeros are determined, the next step is to synthesise poles to control the OOBG. Butterworth type and Chebyshev type II poles are all suitable for the NTF synthesis because they make the magnitude of the transfer function monotonically changing in the NTF passband. Butterworth type poles are uniformly distributed on a circle in the s-plane [46]. However, for the stability criteria, only the LHP poles are selected for the NTF synthesis. The LHP Butterworth type poles are located at

$$p_{ks} = r \cdot e^{j\frac{(2k+M-1)\pi}{2M}}, \qquad (k = 0, 1, \cdots, M-1) \tag{5.29}$$

where M is the order and r is the radius of the circle. Again, Bilinear transformation is applied for the s-plane to z-plane mapping as depicted in Figure 5.11. The poles in the z-domain can be expressed as

$$p_{kz} = \frac{1 + p_{ks}}{1 - p_{ks}}. \tag{5.30}$$

The radius r in Eq. 5.29 is used as a tuning parameter for the OOBG control. According to Lee's rule, the OOBG can range from 1.5 to 2 to keep a safety-margin. For every searching step of r, the magnitude of NTF is calculated at $z = -1$. The searching

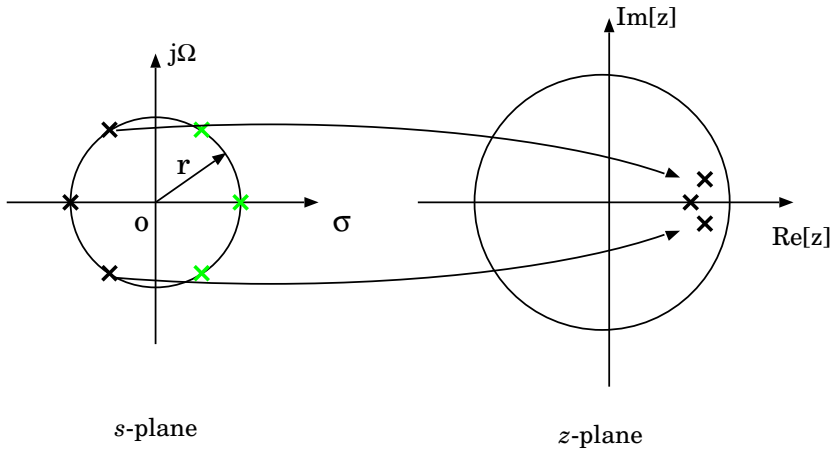


Figure 5.11. Bilinear mapping of the Butterworth poles from the s-plane to the z-plane.

loop is broken when the calculated $|NTF(z)|_{z=-1}$ satisfies the Lee's rule. The flowchart of the pole synthesis is shown in Figure 5.12.

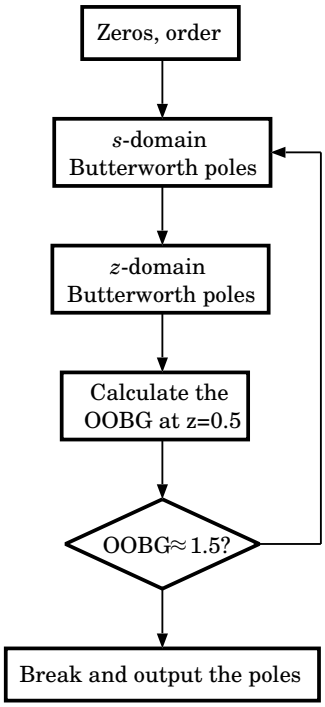


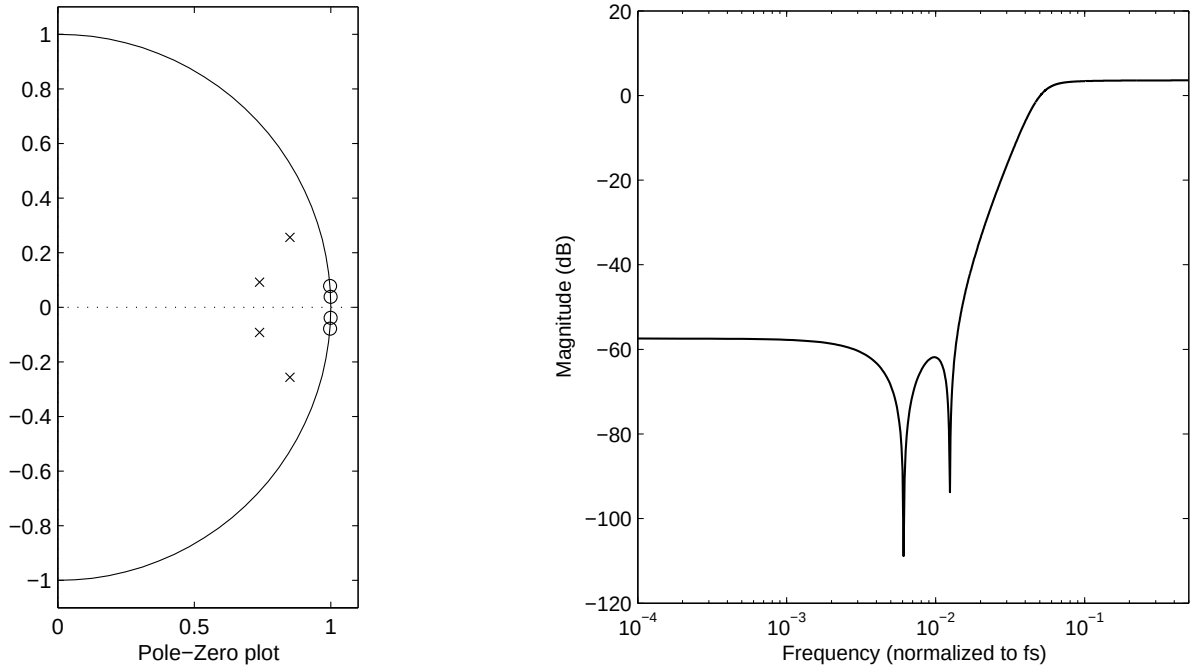
Figure 5.12. Flowchart of the Butterworth type poles synthesis.

When the zeros and the poles are synthesised, an SDM NTF is obtained. As an example, a fourth-order NTF with Chebyshev type II zeros, Butterworth type poles,

OSR=32, and OOBG=1.5 is synthesised as

$$NTF(z) = \frac{(z^2 - 1.999z + 1)(z^2 - 1.994z + 1)}{(z^2 - 1.478z + 0.5548)(z^2 - 1.7z + 0.7879)}. \tag{5.31}$$

The Pole-Zero plot and the NTF magnitude response are plotted in Figure 5.13.



(a) (b)

Figure 5.13. Synthesised 4th-order NTF with OSR=32 and OOBG=1.5. (a) Pole-Zero plot; (b) magnitude response.

5.4 Simulations and Spectrum Analysis

Since none of the stability criteria for the NTF synthesis is adequate, the modulator stability has to be verified using simulations. In addition, the modulator performance, in terms of SNR and DR, can be evaluated by simulations.

5.4.1 Simulations in State-Space

The synthesised NTF can be simulated in so-called state-space [46]. For a discrete LTI system, when the transfer function and the initial state are chosen, then all the future

states of the LTI system can be predicted by

$$\lambda(n+1) = \mathbf{A}\lambda(n) + \mathbf{B}\mathbf{x}(n), \tag{5.32}$$

$$y(n) = \mathbf{C}\lambda(n) + \mathbf{D}\mathbf{x}(n), \tag{5.33}$$

where $\mathbf{x}$ and $\mathbf{y}$ are the input and output vectors respectively, λ is the state variable, which describes the internal state of the LTI system, and $\mathbf{A}(N \times N)$, $\mathbf{B}(N \times M)$, $\mathbf{C}(K \times N)$, $\mathbf{D}(K \times M)$ are the state matrices, where M, N, K are the size of the input, state variable and the output vectors. By taking the z-transform of Eq. 5.32 and Eq. 5.33, and assuming the initial state variable $\lambda(0)$ is 0, the transfer function of the LTI system can be expressed by the state matrices as

$$H(z) = \mathbf{C}(z\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + \mathbf{D}, \tag{5.34}$$

where $\mathbf{I}(N \times N)$ is an identity matrix. In MATLAB, the *ss* function can easily transform the LTI system transfer function to the state-space model.

A general SDM can be separated into a linear TF-filter and a nonlinear quantiser as illustrated in Figure 5.14, when the STF of the SDM is set to 1. The TF-filter has two inputs X, Y and a single output W. The output of the TF-filter at node W can be written as

$$W = (1+H)X - HY = \begin{pmatrix} 1+H & -H \end{pmatrix} \begin{pmatrix} X \\ Y \end{pmatrix} = G \begin{pmatrix} X \\ Y \end{pmatrix}, \tag{5.35}$$

where $H = 1/NTF - 1$ is the loop filter, and $G = (1+H \quad -H)$ is the transfer function of the two-input, single-output TF-filter, which is transformed into state space by MATLAB *ss* function for the simulation. When the state matrices $\mathbf{A}, \mathbf{B}, \mathbf{C}, \mathbf{D}$ of the transfer function G are obtained, the output of the TF-filter W can be calculated using Eqs. 5.32, 5.33, and the quantised output Y is given by sgn$[W]$.

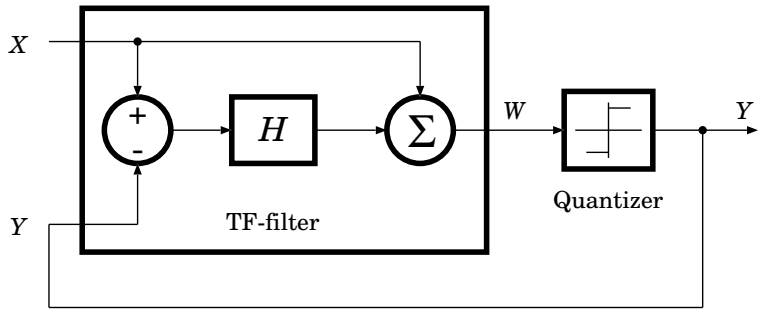


Figure 5.14. Block diagram of a general SDM separated into a linear TF-Filter and a nonlinear quantiser.

For the fourth-order NTF expressed in Eq. 5.31, the state matrices of the TF-filter $G(z)$ can be calculated using MATLAB as

$$\mathbf{A} = \begin{pmatrix} 0 & 0 & 0 & -0.250 \\ 0.5 & 0 & 0 & 0.4991 \\ 0 & 2 & 0 & -1.4965 \\ 0 & 0 & 4 & 3.9930 \end{pmatrix}, \tag{5.36}$$

$$\mathbf{B} = \begin{pmatrix} -0.1407 & 0.1407 \\ 0.2357 & -0.2357 \\ -0.5327 & 0.5327 \\ 0.8150 & -0.8150 \end{pmatrix}, \tag{5.37}$$

$$\mathbf{C} = \begin{pmatrix} 0 & 0 & 0 & 1 \end{pmatrix}, \tag{5.38}$$

$$\mathbf{D} = \begin{pmatrix} 1 & 0 \end{pmatrix}. \tag{5.39}$$

The MATLAB script for the simulation of Figure 5.14 in state-space is shown in Figure 5.15, where "N" is the input data length, "w" is the TF-filter output, "y" is the quantised output and "Lambda" is the state variable. The calculated quantisation noise spectrum and the simulated PSD with a sinusoid input are plotted in Figure 5.16. The two graphics show very good agreement between the estimated and simulated results.

The SNR can be calculated by the signal power divided by the total inband noise power. With different input signal power values, the DR can be obtained from the plot of the SNR versus the input power as shown in Figure 5.17.

```
for i=1:N-1
   w(i)=C*Lambda+D*[x(i); y(i)];

   if (w(i) >= 0)
      y(i)=1;
   else
      y(i)=-1;
   end

   Lambda=A*Lambda+B*[x(i); y(i)];
end
```

Figure 5.15. MATLAB script for SDM simulations in state-space.

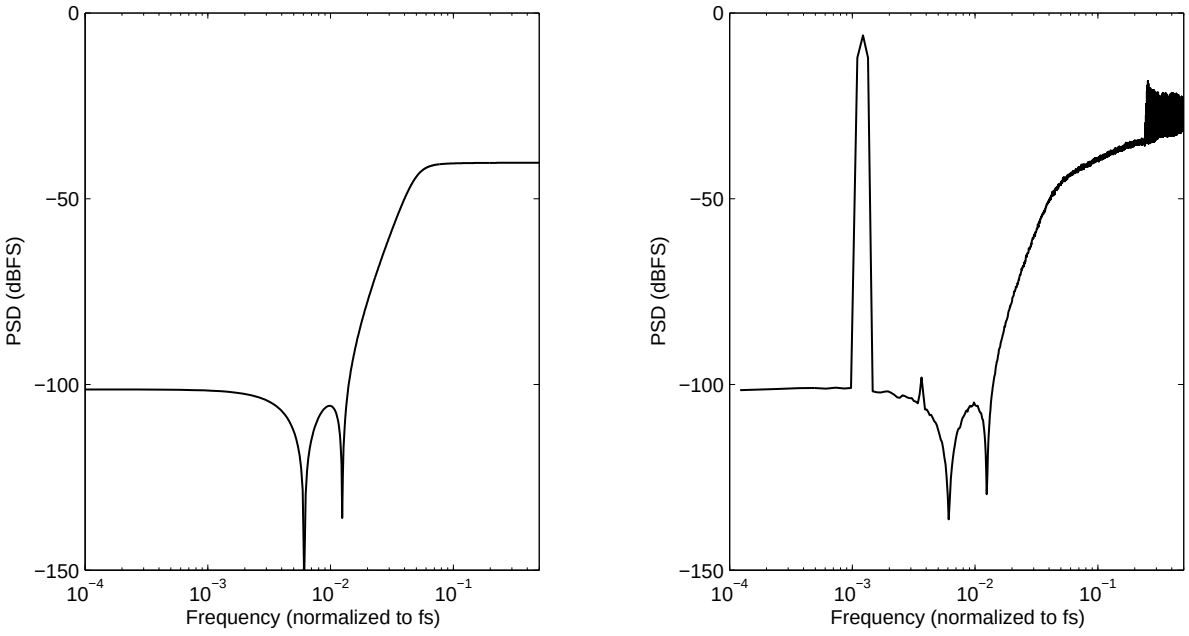


Figure 5.16. (a) Calculated quantisation noise PSD, and (b) simulated PSD of the 4th-order SDM of Eq. 5.31.

5.4.2 Simulations using SIMULINK

In addition to the state-space method, simulations using SIMULINK are very intuitive because the SDM SIMULINK models realise the transfer functions to the topologies, which can be further implemented into circuit building blocks. But due to its slow speed, SIMULINK is not convenient for long time simulations. A good methodology is to evaluate the synthesised SDM transfer function in state-space; then use SIMULINK model as a bridge mapping the transfer function to the circuit building blocks.

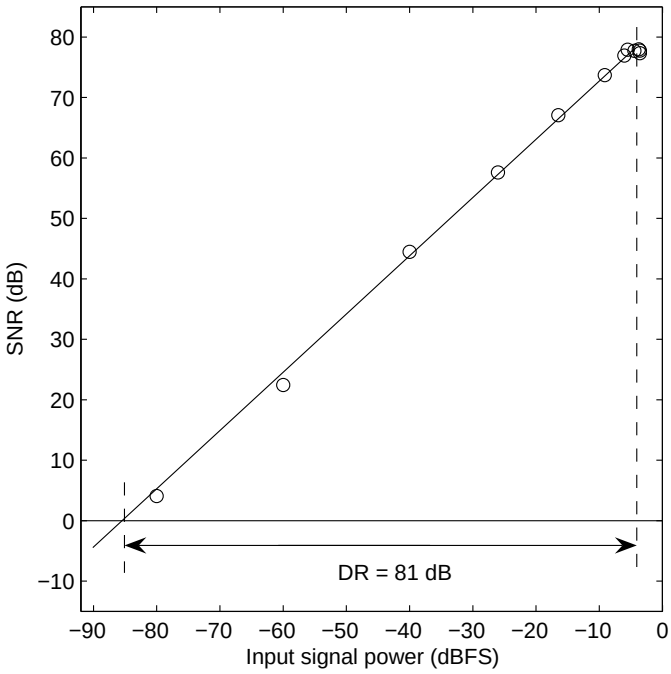


Figure 5.17. Simulated dynamic range of the 4th-order LPSDM with OSR=32.

The criteria of designing a general SDM SIMULINK model is to have enough degrees of freedom to realise the required transfer function. There are several feasible topologies have been developed and included in Scherier's SDM design toolbox [45]. Figure 5.18 illustrates a fourth-order SDM using the CRFB topology. The NTF of the SDM is given by Eq. 5.31 and the STF is set to 1. For the simulation, a sinusoidal signal is fed into the modulator and the output data is then fed to the MATLAB workspace for spectrum analysis. Figure 5.19 shows the output PSD, which is the same as the result simulated in state-space shown in Figure 5.16(b).

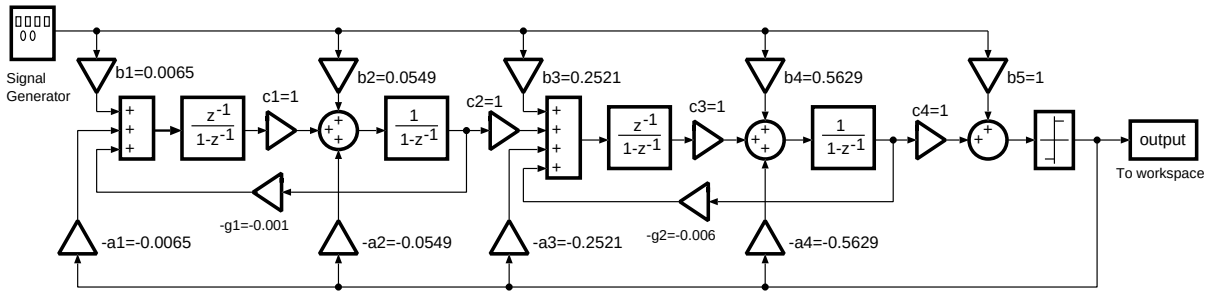


Figure 5.18. SIMULINK model of the 4th-order SDM using the CRFB topology.

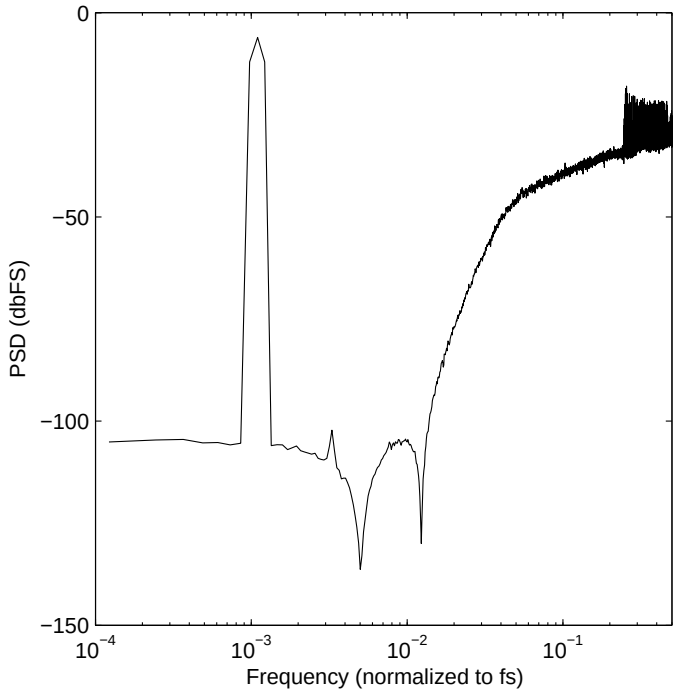


Figure 5.19. PSD of the 4th-order SDM simulated by SIMULINK.

5.4.3 Spectrum Analysis

The available data sequence for spectrum analysis must be limited length. This can be treated as an infinitive data stream selected (multiplied) by a square window in the time domain. This multiplication becomes a convolution between the Fourier transformed data and the window function in the frequency domain. Therefore, the mainlobe of the window function may smear the signal power into the adjacent frequency bins, and the sidelobes of the window function may spread the power, causing spectrum leakage. So that, a favourable window function should have narrow mainlobe and fast decayed sidelobes.

Square window, which is a sinc function in the frequency domain, has very narrow mainlobe, however the strong sidelobes can introduce serious spectrum leakage. The square windowed spectrum of the fourth-order SDM output is shown in Figure 5.20. Compared to Figure 5.16, the ripples of the spectrum due to the NTF shaping inside the signal band is merged into the leaked spectrum and cannot been seen.

Hann window and Blackman window, as plotted in Figure 5.21, are often used for spectrum analysis. Hann window has narrower mainlobe but stronger sidelobes compared with Blackman window. The Hann and Blackman windowed spectrum of the fourth-order

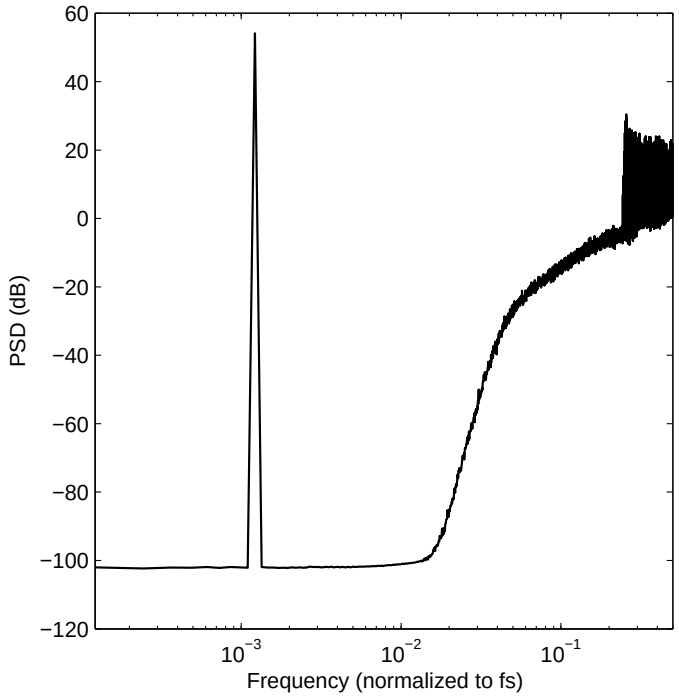
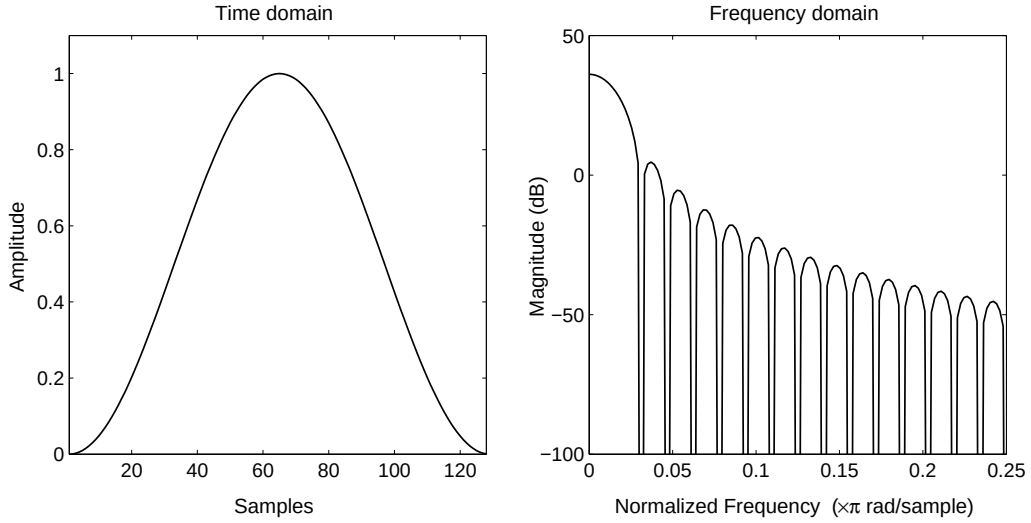


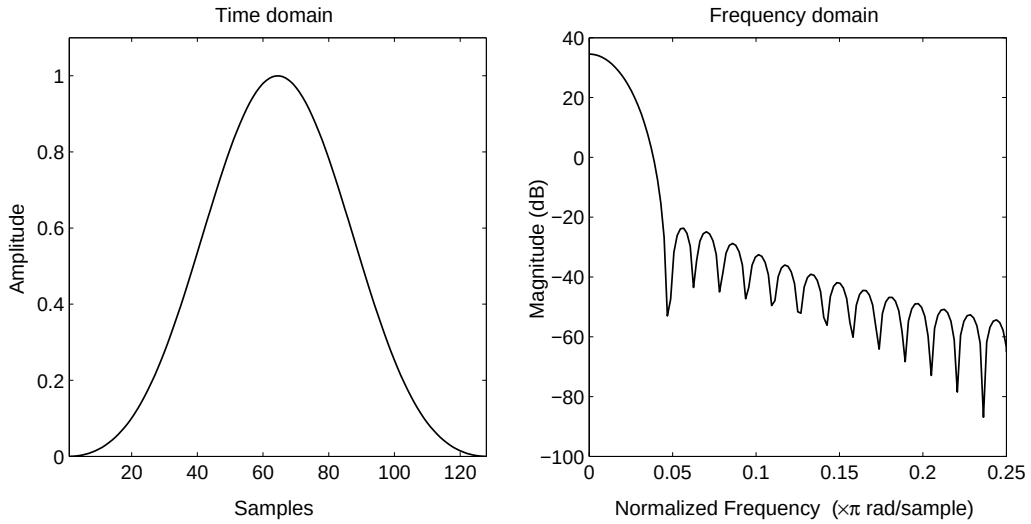
Figure 5.20. PSD of the 4th-order SDM with square windowed output.

SDM output is shown in Figure 5.22. Both of the window functions are able to present the details of the noise shaping, whereas the difference is that the signal power only smears into the adjacent two bins for Hann windowed spectrum and four bins for the Blackman windowed spectrum, due to the different width of the window function mainlobes. This is important when calculating the SNR, because as illustrated in Figure 5.22, three dots represent the signal power and should be removed from the total inband noise power for the Hann windowed spectrum, and five dots for the other one. When the function $calculateSNR$ in Scherier's SDM design toolbox is used for the SNR calculation, Hann window must be applied for the data sequence.

In addition to the application of window functions, the input sinusoidal signal must be located on the frequency bin to avoid signal power splatter. To obtain a physical picture of this issue, we return to the continuous Fourier transform first, and only consider the positive frequency spectrum. An ideal sinusoid with infinitive lenght exhibits a single beat spectrum as $\delta(f - f_{in})$, where f_{in} is the sinusoid frequency. However, only finite data length is practically available for the Fourier transform in experiment. This can be interpreted as an infinitive sinusoid selected by a square window. The resulting spectrum



(a)



(b)

Figure 5.21. (a) Hann and (b) Blackman window functions.

is given by

$$\begin{aligned} S_{ee}(f) &= |\mathcal{F}[\cos(2\pi ft)\cdot \mathrm{rect}(0,\ T)]|^2 \\ &= |\delta(f-f_{in}) * \mathrm{sinc}(\pi fT)|^2 \\ &= \left|\int \delta(\tau - f_{in})\mathrm{sinc}[\pi(f-\tau)T]d\tau\right|^2 \\ &= |\mathrm{sinc}[\pi(f-f_{in})T]|^2\,, \end{aligned} \tag{5.40}$$

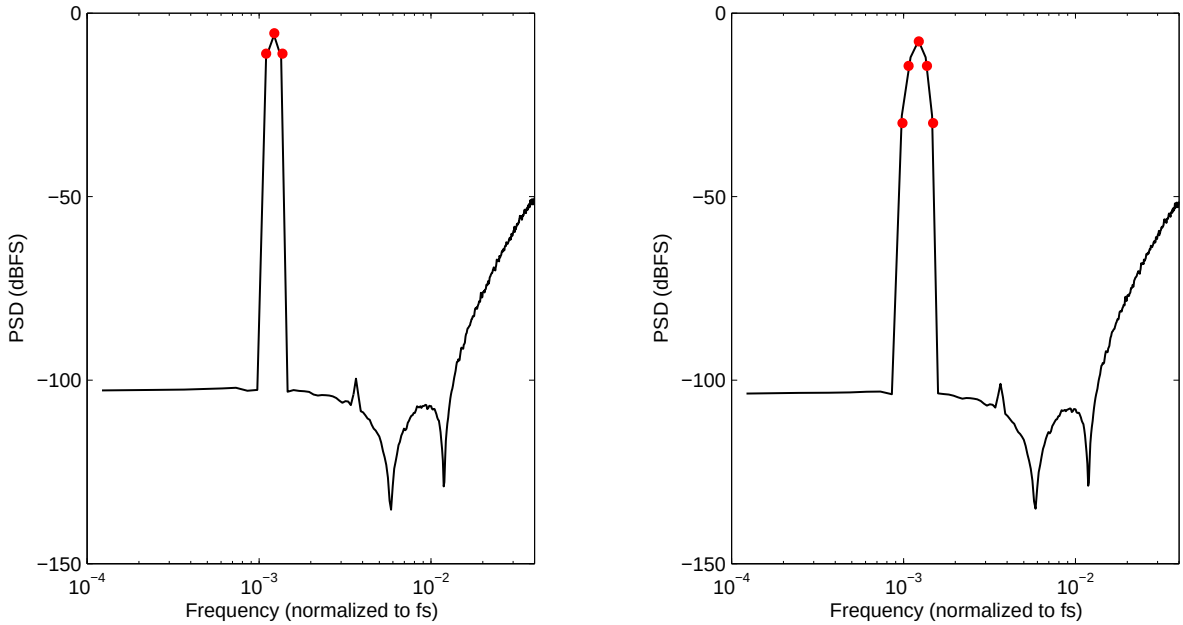


Figure 5.22. PSDs of the 4th-order SDM with (a) Hann windowed and (b) Blackman windowed outputs.

where T is the square window length. Since the realistic data sequence must be discrete, we analyse Eq. 5.40 for discrete frequencies from DC to the sampling frequency f_s. Assuming that the sampled data length is N, the frequency step is Δf, the sampling period is t_s, and representing the input sinusoid frequency as $k(\Delta f)$, where k is not necessarily an integer, Eq. 5.40 can be converted to a discrete format as

$$S_{ee}(n\Delta f) = |sinc[\pi(n-k)(\Delta f)Nt_s]|^2 . \qquad n = 0, 1, \cdots, N-1 \tag{5.41}$$

Spectrum analysis using the DFT technique distributes the power density from DC to the sampling frequency f_s. Thereby we have the relation of

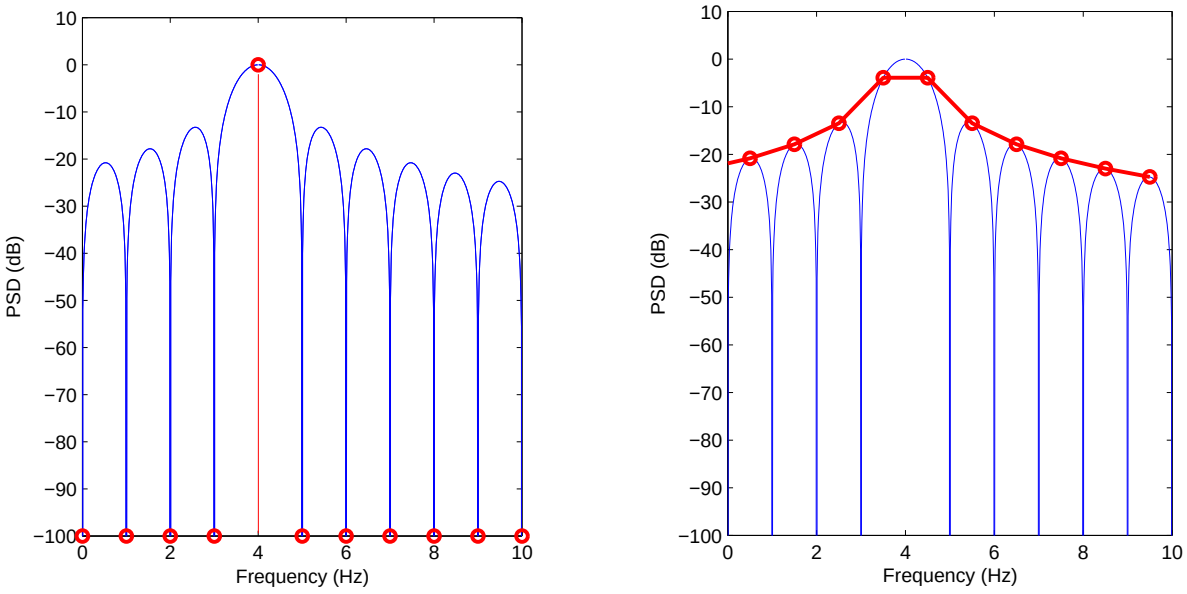
$$f_s = \frac{1}{t_s} = N(\Delta f), \tag{5.42}$$

and therefore Eq. 5.41 can be simplified as

$$S_{ee}(n\Delta f) = |sinc[\pi(n-k)]|^2 . \qquad n = 0, 1, \cdots, N-1 \tag{5.43}$$

When the input sinusoid frequency $k(\Delta f)$ is located on the frequency bin, which means k is an integer, Eq. 5.43 has its signal pulse at $f = k(\Delta f)$ when $n = k$, and nulls at all the other frequency bins when $n \neq k$, resulting in a single-beat spectrum as shown in

Figure 5.23(a). However, if k is not an integer, the sampled sinc function in the frequency domain is miss-aligned, therefore the sidelobes spread the signal power, as illustrated in Figure 5.23(b).



(a) (b)

Figure 5.23. PSD of a discrete sinusoid with the frequency (a) located on the frequency bin, and (b) shifted by 0.5 frequency bin.

If the signal frequency is not located on a frequency bin, even with window functions, such as Hann or Blackman windows, the much smaller sidelobes still can splatter the signal power. The Han windowed PSD of the fourth-order SDM output with miss-aligned input frequency is shown in Figure 5.24. The skirt shaped signal power is problematic for the SNR calculation, because it is difficult to remove the signal power from the inband quantisation noise power.

5.5 Bandpass Sigma-Delta Modulators

In a digital heterodyne receiver, the signal is digitised at the IF rather than at the baseband by a BPSDM ADC, as illustrated in Figure 5.25. The IF to baseband conversion is achieved in the digital domain using digital downconversion techniques.

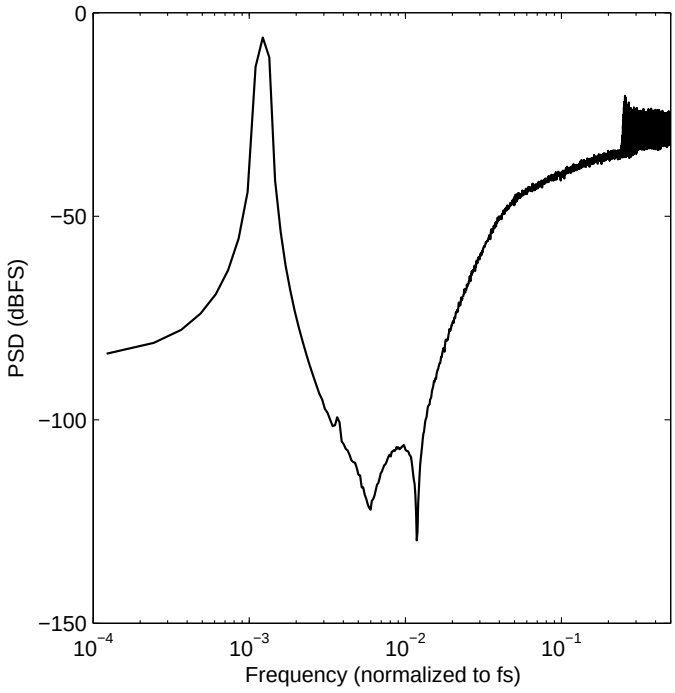


Figure 5.24. PSD of the 4th-order SDM with signal power splatter due to the input sinusoid frequency shifted from the frequency bin.

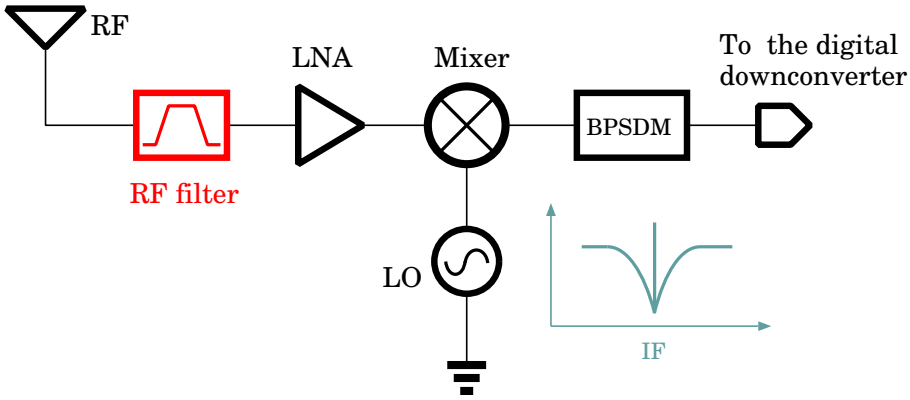


Figure 5.25. Digital downconverter architecture using a BPSDM.

Unlike the noise shaping of an LPSDM, the NTF of a BPSDM is a bandstop filter, which pushes the quantisation noise power towards both high and low frequency regions. To achieve the bandstop noise shaping, the zeros of a BPSDM NTF are put on the unit circle on the z-plane inside the signal band $[2\pi(f_c - f_B/2),\ \ 2\pi(f_c + f_B/2)]$ to form a deep notch, where f_c is the centre frequency and f_B is the passband bandwidth. The OSR of a bandpass SDM is defined as one-half the sampling frequency divided by the passband bandwidth [47], in contrast to the baseband bandwidth of the LPSDM. The STF of a

BPSDM can either be a bandpass or an allpass filter with unity gain. Consequently, the SNR is improved as the signal power is remained the same, while the inband noise power is suppressed. Figure 5.26 shows a typical NTF and a STF of a fourth-order BPSDM.

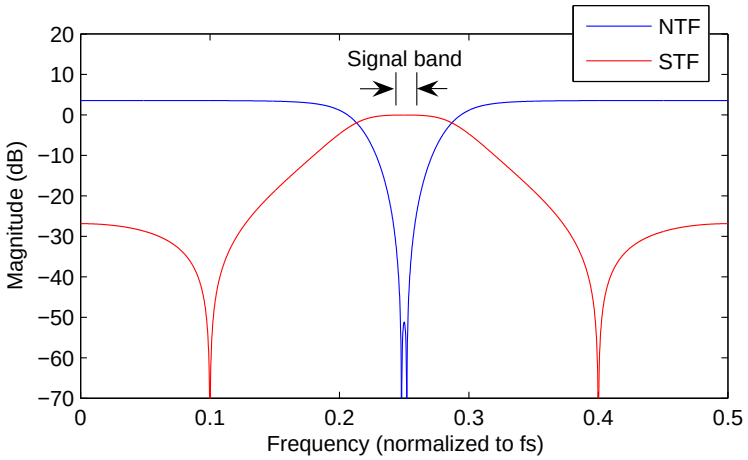


Figure 5.26. NTF and STF of a 4th-order BPSDM.

Similar to the LPSDM NTF synthesis, the design of a BPSDM NTF also needs to satisfy the stability and causality constraints expressed in Eqs. 5.19 and 5.23. Since the noise shaping principle for LPSDMs and BPSDMs are the same except for the centre frequency, the LPSDM NTF synthesis procedures illustrated in Figures 5.10 and 5.12 can also be applied for BPSDM design. The only difference is that the z-plane zeros and poles are rotated to the BPSDM centre frequency $\pm 2\pi f_c$ first, and then tuning for the minimum inband noise power and the OOBG to satisfy Lee's rule-of-thumb, as illustrated in Figure 5.27.

The zeros and poles at $-2\pi f_c$ do not contribute to noise shaping, but merely to form conjugated zero and pole pairs, so that the BPSDM NTF real coefficients are implementable. As a result, to achieve the same noise shaping efficiency, a BPSDM requires the double order of its LPSDM prototype. A fourth-order BPSDM NTF with an OSR of 64 is synthesized by the pole-zero rotation method as

$$NTF(z) = \frac{(z^2 + 0.0252z + 1)(z^2 - 0.0252z + 1)}{(z^2 + 0.3378z + 0.6622)(z^2 - 0.3378z + 0.6622)}. \tag{5.44}$$

If a bandpass filter is chosen for the STF, the SDM model for the simulation in state-space is shown in Figure 5.28. $F(z)$ is the feedthrough filter to realise the STF, given by

$$F(z) = STF(z) + H(z)[STF(z) - 1]. \tag{5.45}$$

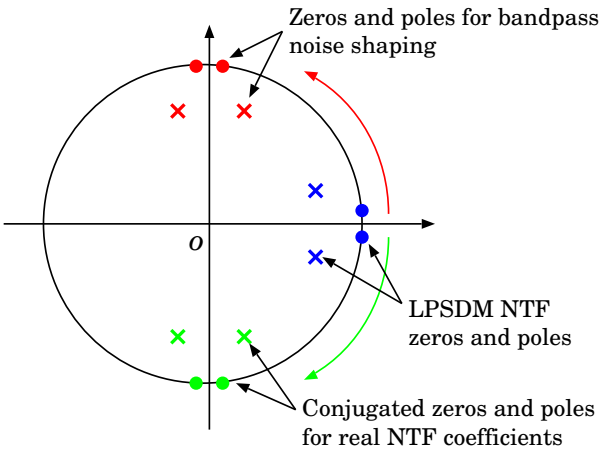


Figure 5.27. NTF synthesis of a BPSDM by tuning the zeros and poles at the centre frequency.

The two-input, single-output TF-filter $G(z)$ can be written as

$$G(z) = (H + F \quad -H). \tag{5.46}$$

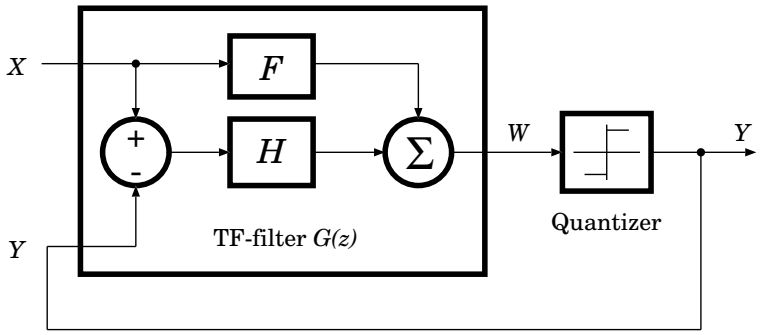


Figure 5.28. Block diagram of a general SDM separated into a linear TF-filter including two filters H and F, and a non-linear quantiser.

The STF share the same poles with the NTF [48], whereas the zeros of the STF are put in the NTF passband on the unit circle to form a bandpass filter action for the input signal. The STF for the fourth-order BPSDM is synthesised as

$$STF(z) = \frac{0.087(z^2 - 1.618z + 1)(z^2 + 1.618z + 1)}{(z^2 - 0.3378z + 0.6622)(z^2 + 0.3378z + 0.6622)}. \tag{5.47}$$

The STF and NTF pole-zero plots are shown in Figure 5.29 and the magnitude responses are illustrated in Figure 5.26.

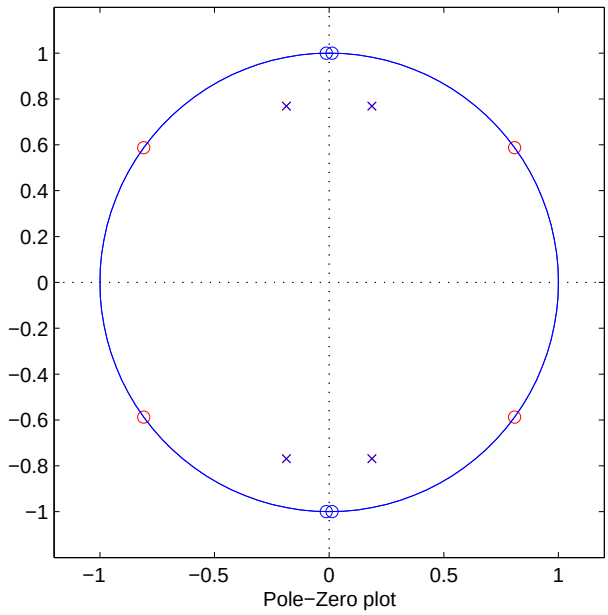


Figure 5.29. Pole-zero plot of the NTF and STF of the synthesised BPSDM. The STF, NTF share the same poles; the NTF zeros are in blue and the STF zeros are in red.

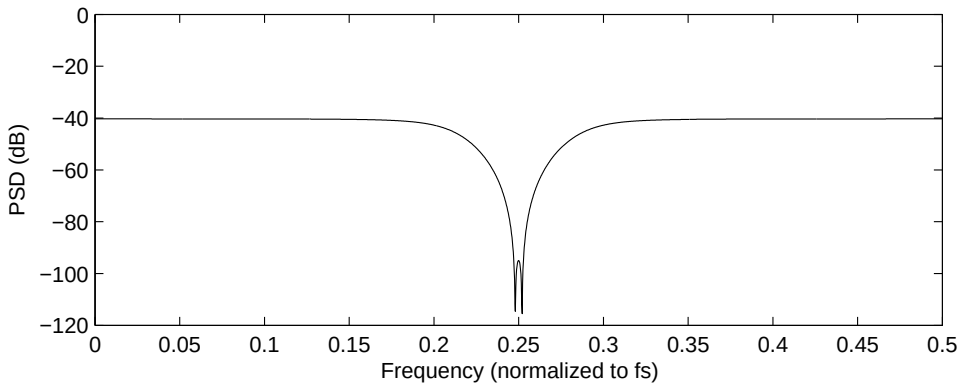
Based on the synthesised STF and NTF, the TF-filter $G(z)$ of the BPSDM is derived as

$$G(z) = \begin{pmatrix} \frac{0.087(z^2+1)(z^2+7.452)}{(z^2+0.0251z+1)(z^2-0.0251z+1)} \\ \frac{0.7891(z^2+0.7116)}{(z^2+0.0252z+1)(z^2-0.0252z+1)} \end{pmatrix}^{\top}. \tag{5.48}$$

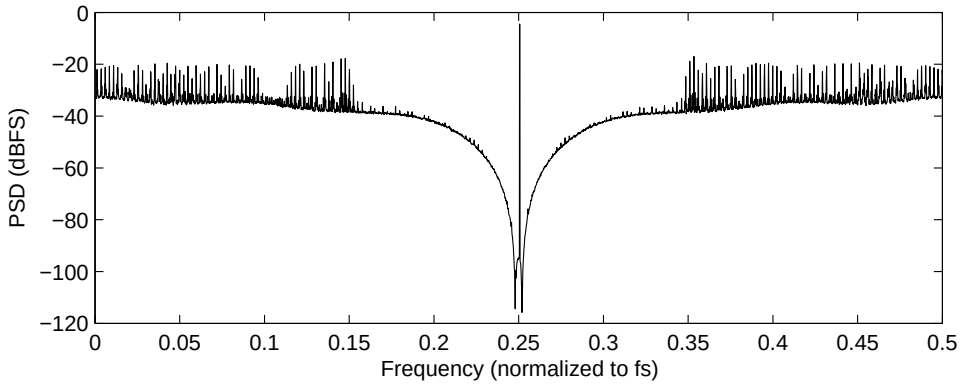
By transforming $G(z)$ into state-space, the simulation of a BPSDM can be carried out. The estimated quantisation noise spectrum and the simulated PSD of the fourth-order BPSDM are shown in Figure 5.30. The SNR of the BPSDM can be calculated as the signal power divided by the total noise power inside $[f_c - 1/2f_B, \quad f_c + 1/2f_B]$. Similiar to that of the LPSDM, the DR is then obtained by plotting the SNR versus the input signal power as illustrated in Figure 5.31.

The NTF and the STF of the fourth-order BPSDM also can be mapped to the CRFB topology shown in Figure 5.18, yielding the following coefficients

$$\begin{aligned} a &= [-0.2417 \;\; 0.0142 \;\; -0.5615 \;\; 0.5615], \\ b &= [-0.2417 \;\; 0.0142 \;\; -0.5615 \;\; 0.5615 \;\; 1], \\ c &= [1 \;\; 1 \;\; 1 \;\; 1], \\ g &= [1.9748 \;\; 2.0252]. \end{aligned} \tag{5.49}$$



(a)



(b)

Figure 5.30. (a) Estimated quantisation noise spectrum, and (b) simulated PSD of the 4th-order BPSDM of Eq. 5.44.

Simulations using the SIMULINK CRFB model give the same results as those done in state-space.

5.6 Variable Centre Frequency Bandpass Sigma-Delta Modulators

In some radio systems, there is a need to sweep the centre frequency of a bandpass data converter to detect a broadcast or adapt to different standards. Hence there is a need to design BPSDMs with variable centre frequencies.

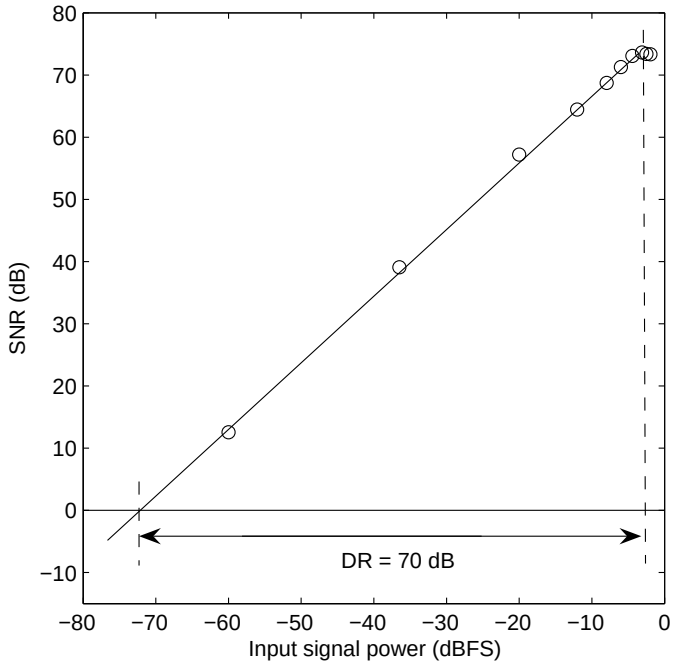


Figure 5.31. Simulated dynamic range of the 4th-order BPSDM with OSR=64.

The centre frequency tuning of a BPSDM can be achieved by rotating the NTF zeros and poles, as illustrated in Figure 5.32. Rotating the pole-zero location by ω degrees on the z-plane shifts the NTF magnitude response by $\omega/2\pi$ without changing the notch shape in the frequency domain, thereby the SNR remains constant when keeping the same OSR. Unfortunately, direct implementation of this approach is difficult, because all the parameters in the topology must be tunable in order to rotate the NTF zeros and poles following a particular relation. Therefore a feasible approach for the VCF modulator is required.

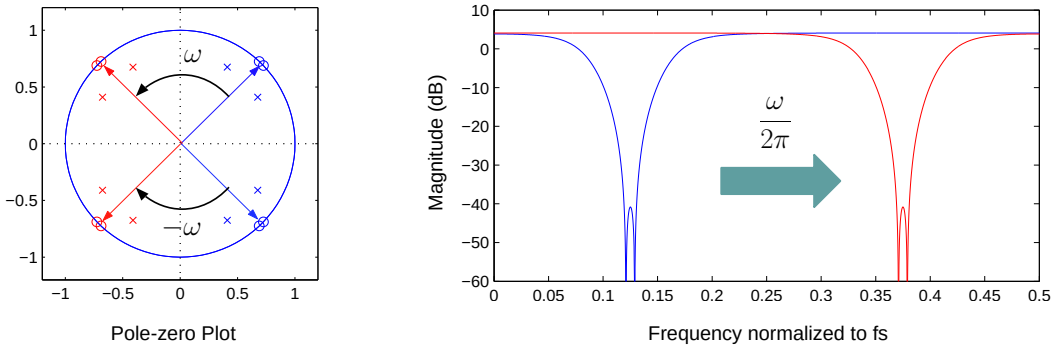


Figure 5.32. BPSDM centre frequency tuning by rotating the NTF zeros and poles.

In the literature, early work on VCF BPSDMs using CT loop filters have been reported [49][50]. However, as will be discussed in the next section, a CT SDM is a combined z and s-domain system, which makes it difficult to analyse the modulator's NTF directly. The designs in [49] and [50] didn't explain the control of the NTF when tuning the modulator centre frequency. An uncontrollable NTF of a VCF BPSDM challenges the modulator stability and noise shaping efficiency, hence the modulator order and performance are limited.

In [51], the author first demonstrated a novel VCF BPSDM algorithm with a controllable DT NTF through all the frequency tuning range by only one parameter. Later a similar approach was reported in [52] and implemented in [53]. In this section, a more detailed analysis in [51] is first presented, then a complete design flow is provided followed by the circuit realisation and measurement.

The NTF of a BPSDM can also be derived by the direct mapping of a LPSDM NTF using [47]

$$z \rightarrow z\frac{z+a}{az+1}; \tag{5.50}$$

where $a \in (-1, 1)$ is the centre frequency tuning parameter. By using Eq. 5.50, a first-order LPSDM integrator loop filter $H(z) = 1/(z-1)$ is mapped to a second-order BPSDM resonator loop filter as

$$R(z) = -\frac{az+1}{z^2+2az+1}. \tag{5.51}$$

The resonator expressed in Eq. 5.51 can be realised into two different topologies as shown in Figure 5.33. Both of these implementations provide an adjustable resonator by tuning the parameter a between -1 and 1, resulting in the corresponding resonance frequency changing from DC to half of the sampling frequency.

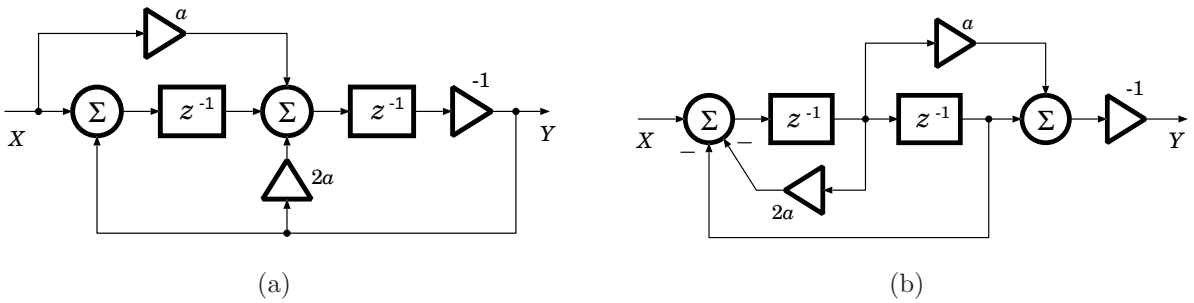


Figure 5.33. Topologies of the VCF resonator.

Figure 5.34 presents the magnitude response of Eq. 5.51 using different values for a. From the plot we can find that the overall shape of $|R(z)|$ does change for different values of a. However, the the resonance peak profiles slightly vary, so that the effect of noise shaping around the signal band is similar when changing the centre frequencies. Therefore, for a narrow band or a large OSR bandpass data conversion, the SNR is expected to have small variance.

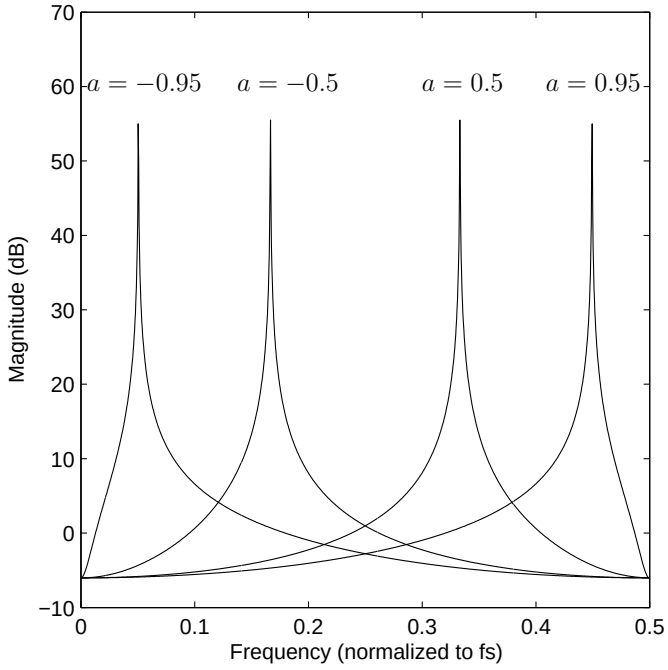


Figure 5.34. The magnitude response of R(z) with different values of a.

Moreover, the magnitude of $R(z)$ monotonically changes out of the signal band, with the same minimum values at DC and 0.5 (normalised frequency). This feature provides a controllable OOBG of the NTF to satisfy Lee's rule of stability, when changing the BPSDM centre frequency.

The resonator architecture, shown in Figure 5.33(a), can be implemented using a fully differential switched-capacitor circuitry as illustrated in Figure 5.35. Longo's unit delay structure [54] is used to realise the resonator. A two-phase clock with phase labelled as '1' and '2' in the schematic diagram controls the unit delay and feedback paths. The resonance frequency is tuned using variable capacitor elements. The feedback paths are

controlled by switchers $Sa+$ and Sa-, corresponding to positive and negative a respectively. This resonator is used to design a fully differential fourth order VCF BPSDM as described in the next paragraph.

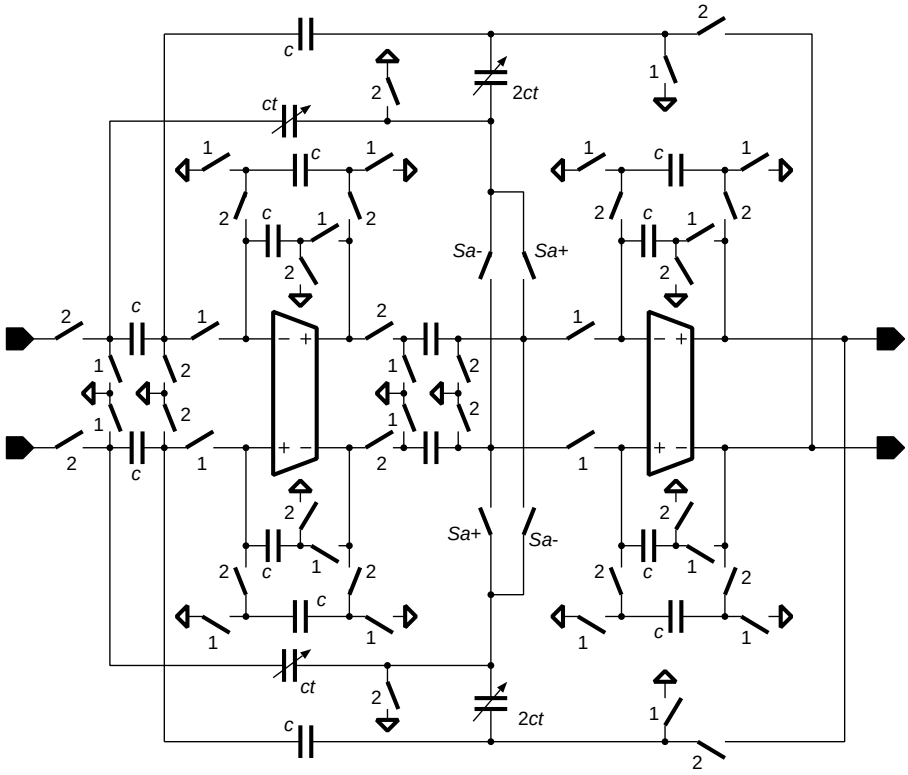


Figure 5.35. Switched-capacitor circuitry realisation of the resonator shown in Figure 5.33(a).

The VCF BPSDM design procedure starts by firstly synthesising a stable and causal NTF, and then realise the NTF using the variable frequency resonator $R(z)$. A fourth-order NTF with Butterworth zeros and poles is synthesised as

$$NTF(z) = \frac{(z^2+1)^2}{z^4 + 1.225z^2 + 0.4414}. \tag{5.52}$$

The next step is to map Eq. 5.52 to a fourth-order BPSDM topology using the resonator $R(z)$, as illustrated in Figure 5.36. The parameters c_1 and c_2 provide two degrees of freedom to achieve the required NTF. Using the linear model of the quantiser, the NTF of the fourth-order BPSDM can be written as

$$NTF(z) = \frac{(z^2-2az+1)^2}{(z^2+2az+1)^2 + c_1c_2(az+1)^2 - c_2(az+1)(z^2+2az+1)}. \tag{5.53}$$

As discussed earlier that the minimum magnitude of $R(z)$ at DC and 0.5 (normalised frequency) is constant regardless the tuning parameter a, we can expect that the OOBG

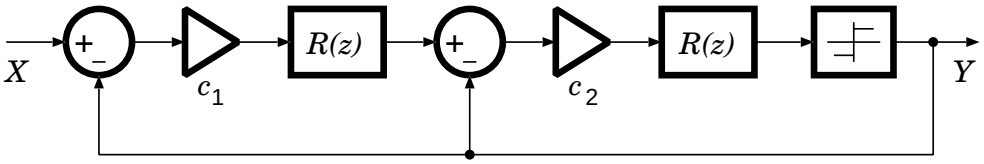


Figure 5.36. Topology of a 4th-order BPSDM with the resonator of Eq. 5.51.

of the NTF is also independent with a. Consequently, it is convenient to set $a = 0$ to calculate c_1 and c_2 while still satisfying Lee's stability rule. The NTF with $a = 0$ is given by

$$NTF(z) = \frac{(z^2+1)^2}{z^4 + (2-c_2)z^2 + 1 + c_1c_2 - c_2}. \tag{5.54}$$

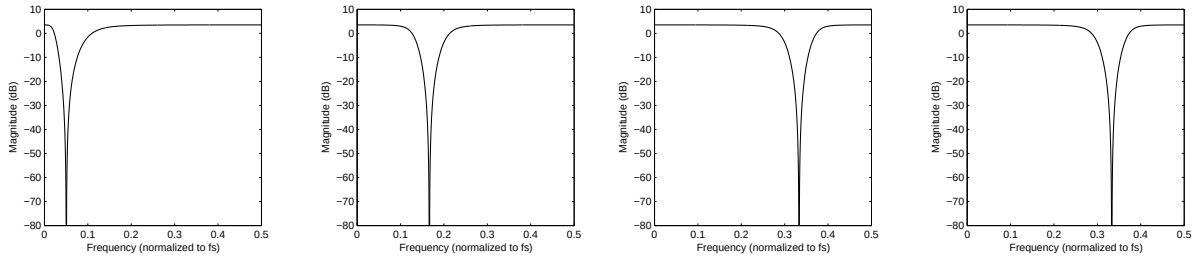
Comparing Eq. 5.52 to Eq. 5.54 and solving for c_1 and c_2 yields

$$[c_1,\ c_2] = [0.2792,\ 0.775]. \tag{5.55}$$

Substitute the coefficients c_1 and c_2 into Eq. 5.53 resulting in the final NTF of the fourth-order VCF BPSDM as

$$NTF(z) = \frac{(z^2-2az+1)^2}{(z^2+2az+1)^2 + 0.21638(az+1)^2 - 0.775(az+1)(z^2+2az+1)}. \tag{5.56}$$

The simulated magnitude responses of Eq. 5.56 with different values of a are shown in Figure 5.37. As expected, the OOBG is in independent of a and remains constant of 1.5 (3.5 dB) at DC and 0.5 (normalised frequency). Hence, Lee's rule for stability is always satisfied when tuning the centre frequency.



(a) a=-0.95 (b) a=-0.5 (c) a=0.5 (d) a=0.95

Figure 5.37. Magnitude response of the VCF NTF with different values of a.

The simulated NTF centre frequency as a function of a is plotted in Figure 5.38. The simulation shows that the centre frequency of the NTF has a nearly linear relation with a, when a ranges between -0.6 and 0.6, but has a curved dependence outside this range. This matter has to be taken into consideration when tuning the modulator.

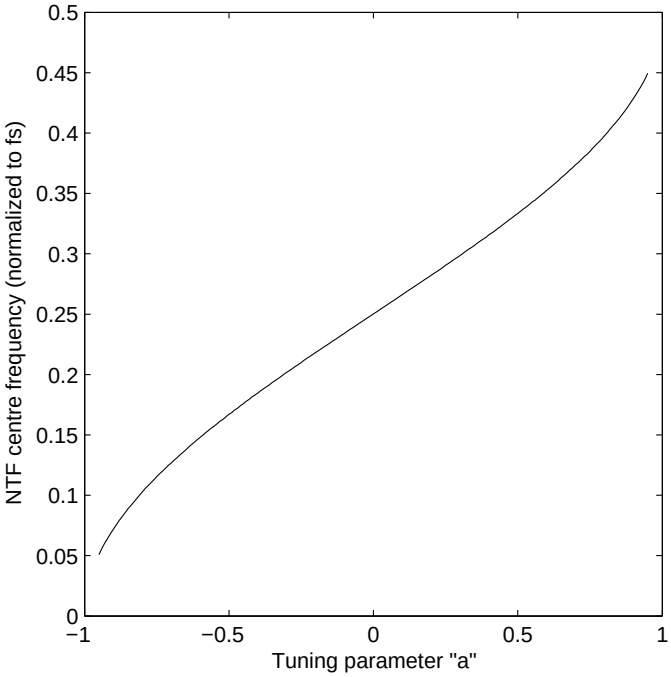
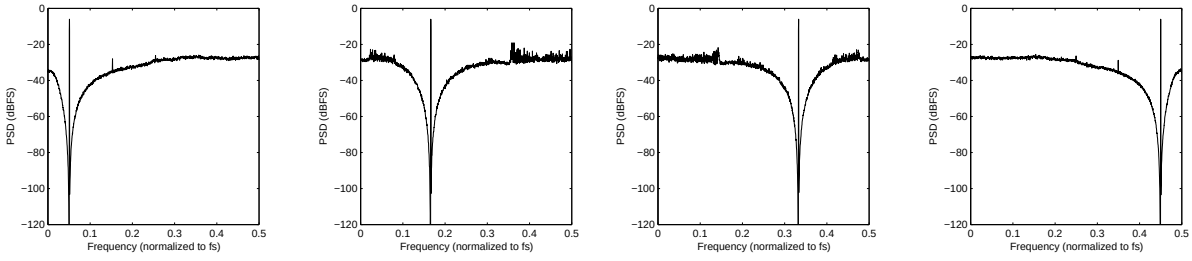


Figure 5.38. The centre frequency of the VCF NTF Vs. a.

The fourth-order VCF BPSDM can be simulated using the state-space method. The NTF centre frequency for a particular value of a should be found first according to Figure 5.38. Then the NTF is transformed into the state-space matrices and simulated with a sinusoidal input signal around the centre frequency. Figure 5.39 presents Hann windowed output spectrums with different values of a. The modulator remains stable throughout the tuning range of a from -0.95 to +0.95, corresponding to the normalised centre frequency changing from 0.05 up to 0.45.

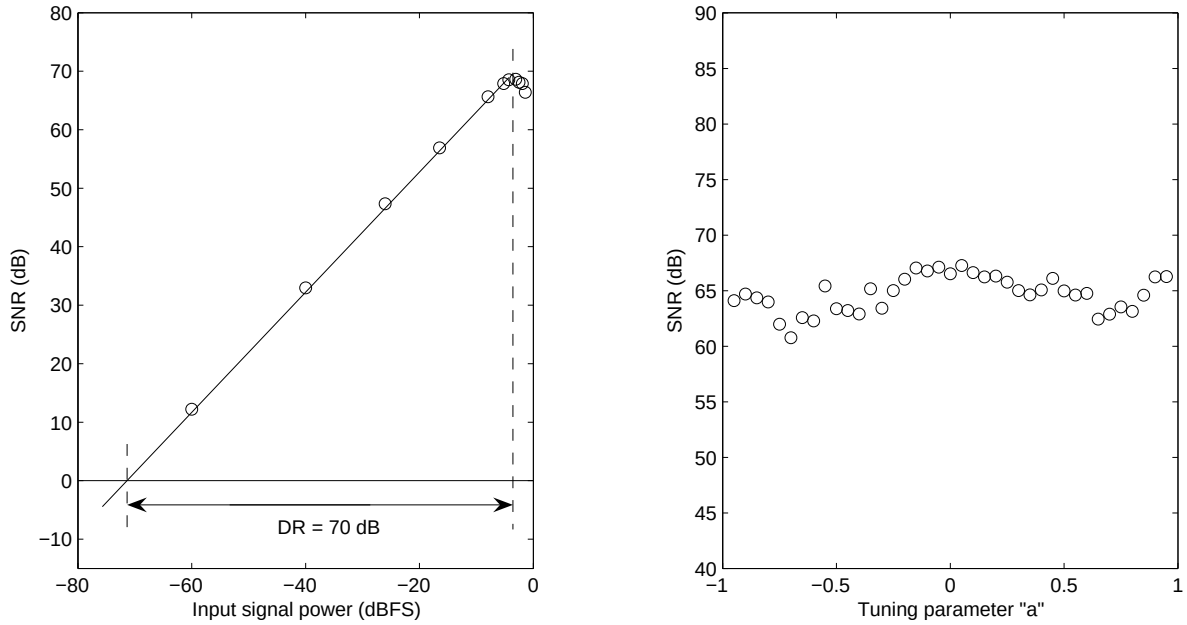


(a) a=-0.95 (b) a=-0.5 (c) a=0.5 (d) a=0.95

Figure 5.39. Output spectrum of the VCF 4th-order BPSDM with different value of a.

The SNR is calculated from the output PSD at an OSR of 64. By calculating the SNR with different input signal power, the DR of the VCF modulator can be obtained

as shown in Figure 5.40(a) while the tuning parameter a is set to -0.95. The SNR varies between 60 dB and 70 dB with an input sinusoidal signal that has one-half full scale amplitude, as illustrated in Figure 5.40(b).



(a) (b)

Figure 5.40. (a) Simulated dynamic range with a=-0.95; (b) SNR Vs. a with an input sinusoid that has one-half full scale amplitude.

The circuit realisation of the fourth-order VCF BPSDM is shown in Figure 5.41 using the switched-capacitor technique. Two extra OTAs are required for the subtraction between the input and the feedback signals before fed into the resonators. The values of a, c_1 and c_2 are realised using the ratios of capacitances.

The tuning range of the modulator is limited by the variable capacitance. In some applications when continuous tuning is not required, the variable capacitors can be replaced by capacitor arrays controlled by combinational logic that selects the desired centre frequency, as illustrated in Figure 5.42.

The design shown in Figure 5.41 has been implemented using the AMI 1.5 µm CMOS process. The SPICE models for the circuit simulation are listed in Appendix A. All the NMOS and PMOS process corners are covered by simulations to ensure a stable modulator. The modulator layout and microphotograph are shown in Figure 5.43. The complete

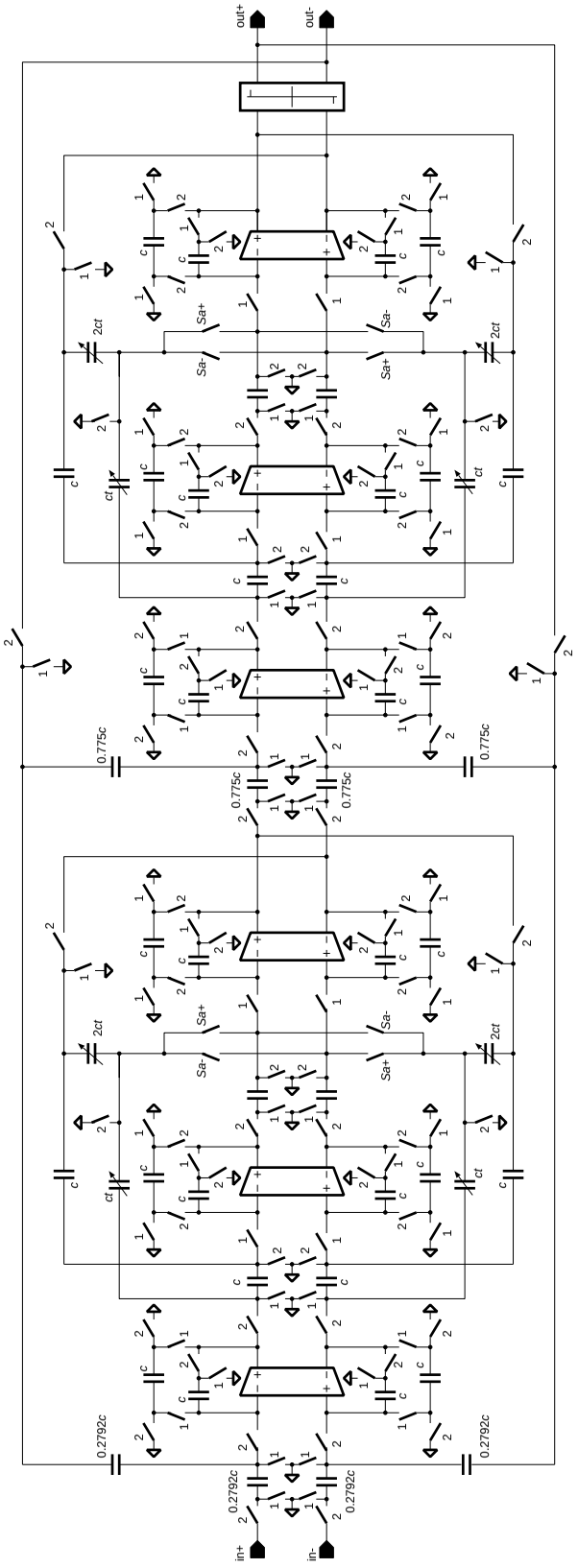


Figure 5.41. Circuit realisation of the 4th-order VCF BPSDM using switched-capacitor technique.

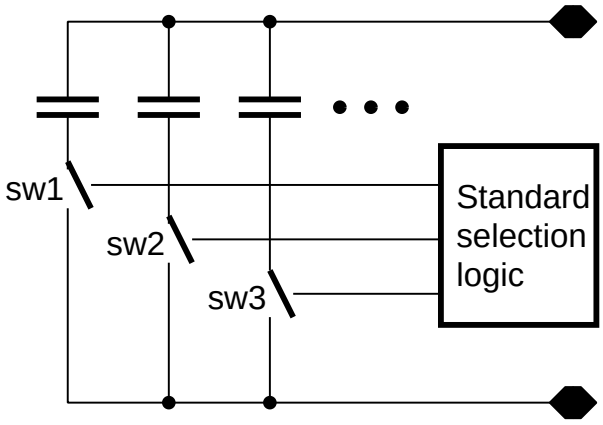
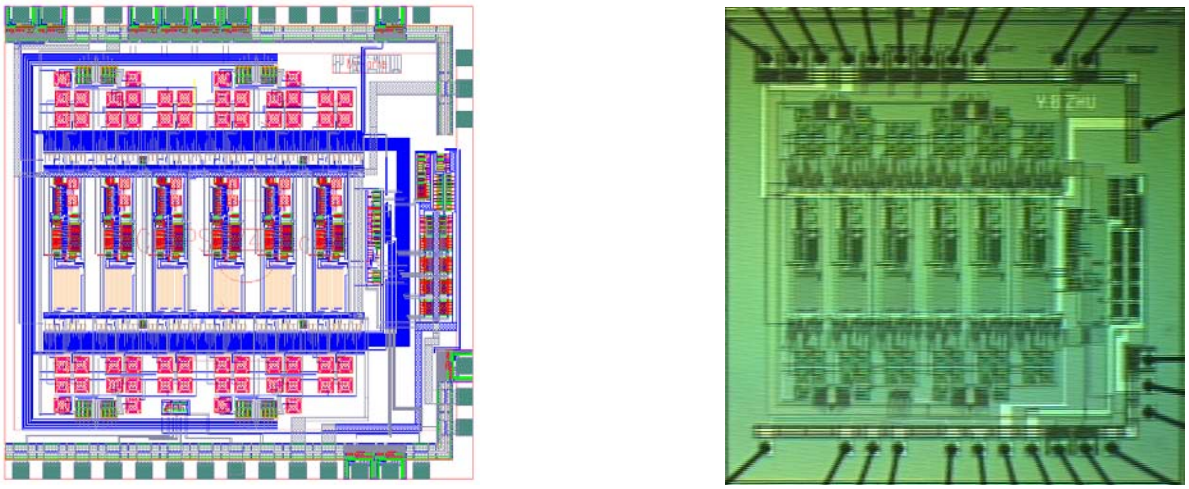


Figure 5.42. Capacitor array for the discrete centre frequency selection.

modulator contains six cascaded unity delay cells, a single-bit quantizer, switch and capacitor arrays, and a non-overlapped differential clock generator. The centre frequency is tuned by a 4-bit control word that provides total 9 different centre frequencies, distributed between 0.1 and 0.4 normalised frequencies.



(a) (b)

Figure 5.43. (a) Layout and (b) microphotograph of the 4th-order VCF BPSDM implemented in a 1.5 µm CMOS process.

The fabricated chip operates at 1 MHz sampling frequency, and drains 40 mA current from ±2.5 V voltage supplies. The measured output spectrums at the nine different centre frequencies are shown in Figure 5.44. The correct quantisation noise shaping validates the algorithm and design methodology. The maximum SNR and DR are 57 dB and 58

dB respectively, measured from the output spectrum at a centre frequency of 350 kHz and an OSR of 64, as shown in Figure 5.45.

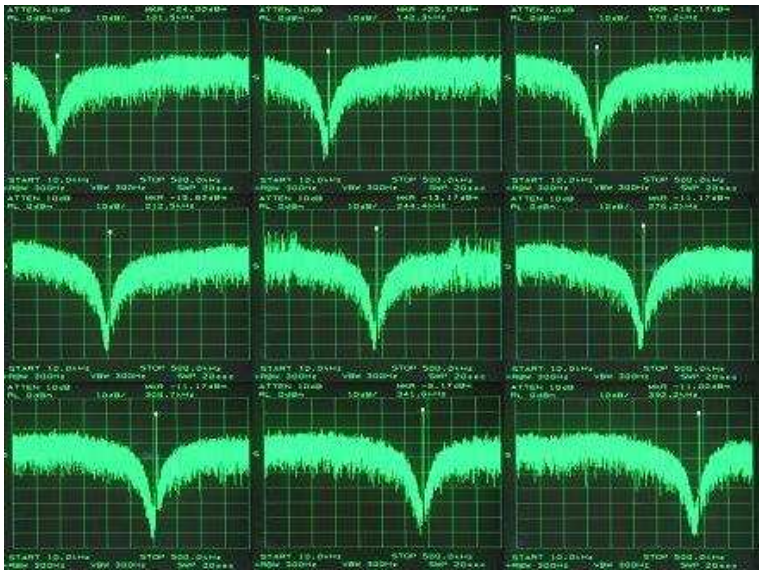


Figure 5.44. Measured PSDs of the 4th-order VCF BPSDM at 9 different centre frequencies.

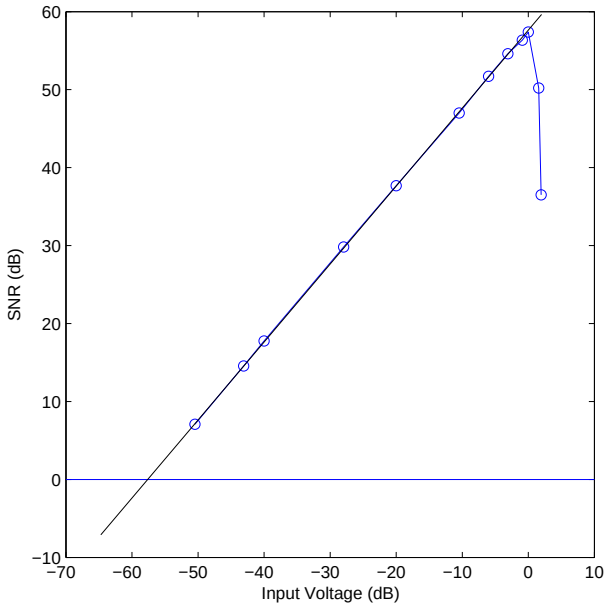


Figure 5.45. Measured DR of the 4th-order VCF BPSDM at a centre frequency of 350 kHz.

5.7 Continuous-Time Sigma Delta Modulators

Not only DT, but also CT filters are suitable for the SDM design. A typical CT SDM consists of a CT loop filter, a sampling quantiser and a feedback DAC, as shown in Figure 5.46. In fact, a CT SDM is a combined DT and CT system, which makes it difficult to be analysed either in the z-domain or in the s-domain. The design procedure of a CT SDM is separated into firstly synthesising a prototype DT loop filter, and secondly transforming the DT prototype into its equivalent CT counterpart.

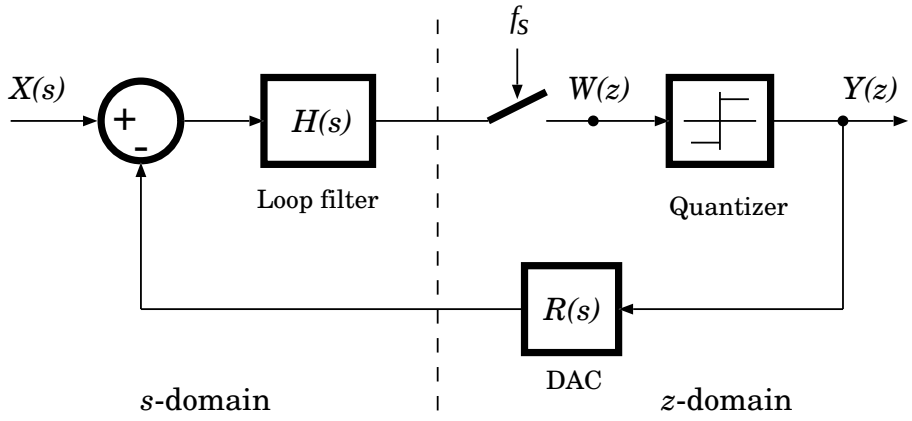


Figure 5.46. Architecture of a CT SDM.

A CT SDM is defined as equivalent to a DT SDM if for the same input signals, the inputs to the quantisers of the two modulators are the same at the sampling instants [55], and thereby the two quantiser will generate exactly the same output bit streams. This definition of the DT to CT conversion is named impulse invariant transformation, which can be expressed mathematically as

$$\mathcal{Z}^{-1}\{H(z)\} = \mathcal{L}^{-1}\{R(s)H(s)\}|_{t=nTs}, \tag{5.57}$$

where $H(z)$ is the DT loop filter, $H(s)$ is the CT loop filter and $R(s)$ is the transfer function of the DAC. NRZ and RZ DAC pulses are often used in the SDM design, as shown in Figure 5.47, where $T_s = 1/f_s$ is the sampling period. The corresponding transfer functions of the NRZ and RZ pulses in the s-domain can be derived using the Laplace transform of rectangular waveforms as

$$R(s) = \begin{cases} \frac{1-e^{-sT_s}}{s}, & \text{NRZ} \\ \frac{1-e^{-0.5sT_s}}{s}. & \text{RZ} \end{cases} \tag{5.58}$$

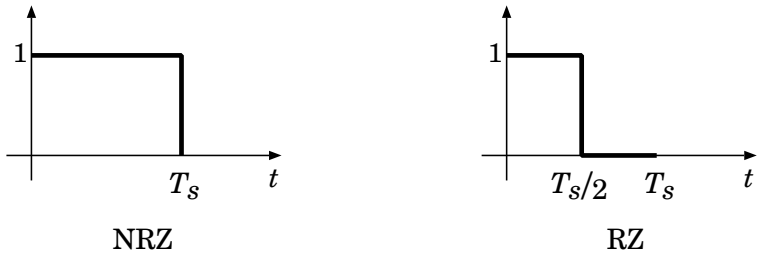


Figure 5.47. NRZ and RZ DAC pulses.

Without loss of generality, the quantiser sampling period T_s is set to 1 sec for the following derivation in this section. For an arbitrary sampling period, the transfer function $H(s)$ can be obtained by transforming s to sT_s.

5.7.1 CT SDM with NRZ DAC Pulse

The sample and hold period of an NRZ DAC pulse is equal to the quantiser sampling period T_s. Therefore Eq. 5.57 can be solved by the z-transform of a CT transfer function. The transfer function of a CT SDM $G(s)$ is given by

$$G(s) = H(s)R(s) = H(s)\frac{1-e^{-s}}{s}. \tag{5.59}$$

By applying the z-transform on both side of Eq. 5.59, $G(s)$ can be expressed in the z-domain as

$$\begin{aligned} \hat{G}(z) &= \mathcal{Z}[G(s)] \\ &= \mathcal{Z}\left[\frac{H(s)}{s}\right] + \mathcal{Z}\left[\frac{e^{-s}H(s)}{s}\right] \\ &= \left(1-z^{-1}\right)\mathcal{Z}\left[\frac{H(s)}{s}\right]. \end{aligned} \tag{5.60}$$

When a CT SDM is equivalent to the DT counterpart, $\hat{G}(z)$ should be equal to the DT loop filter $H(z)$. Then by solving Eq. 5.60, $H(s)$ is obtained.

Example: The loop filter of a second order DT LPSDM is synthesised as

$$H(z) = \frac{0.886z - 0.614}{z^2 - 2z + 1}. \tag{5.61}$$

The topology shown in Figure 5.48 is chosen for the CT SDM design. The loop filter transfer function is given by

$$H(s) = \frac{b_0 s^2 + b_1 s + b_2}{s^2}. \tag{5.62}$$

Then the transfer function along the loop in the z-domain can be expressed as

$$\begin{aligned} \hat{G}(z) &= \mathcal{Z}[G(s)] = \mathcal{Z}[H(s)R(s)] \\ &= \left(1 - z^{-1}\right) \mathcal{Z}\left[\frac{b_0 s^2 + b_1 s + b_2}{s^3}\right]. \end{aligned} \tag{5.63}$$

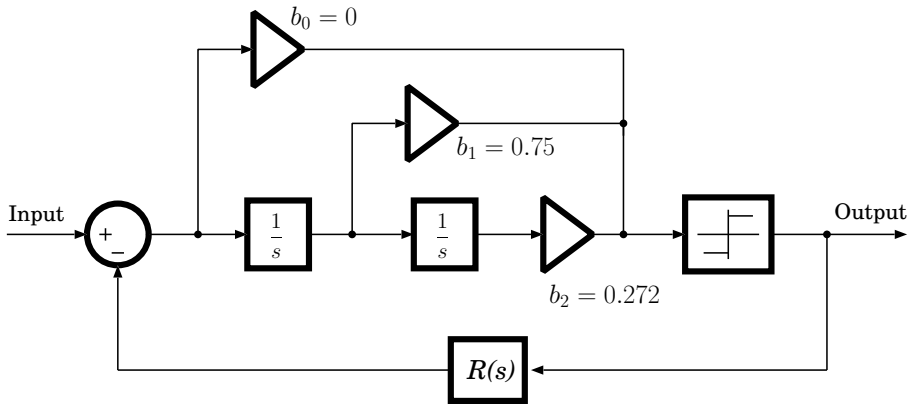


Figure 5.48. Topology of a 2nd-order CT LPSDM.

Symbolic tools, such as MAPLE or MATHEMATICA, can be used to solve Eq. 5.63 yielding

$$\hat{G}(z) = \frac{b_0 - b_1 + b_2 - (2b_0 - b_1 - 0.5b_2)z + 2b_0 z^2}{z^2 - 2z + 1}. \tag{5.64}$$

Equating powers of z in the numerators of Eq. 5.61 and Eq. 5.64, yields the coefficients $[b_0,\, b_1,\, b_2]$ as $[0,\, 0.75,\, 0.272]$, and hence $H(s)$ as

$$H(s) = \frac{0.75s + 0.272}{s^2}. \tag{5.65}$$

Figure 5.49 presents the MATHEMATICA code for the DT to CT conversion. □

The DT to CT conversion with a NRZ DAC pulse shape can also be achieved in state-space by [55]

$$\mathbf{A_c} = \log(\mathbf{A_d}), \tag{5.66}$$

$$\mathbf{B_c} = (\mathbf{A_d} - \mathbf{I})^{-1}\mathbf{A_c}\mathbf{B_d}, \tag{5.67}$$

$$\mathbf{C_c} = \mathbf{C_d}, \tag{5.68}$$

$$\mathbf{D_c} = \mathbf{D_d}, \tag{5.69}$$

where $\mathbf{I}$ is the identity matrix and $[\mathbf{A_d},\ \mathbf{B_d},\ \mathbf{C_d},\ \mathbf{D_d}]$, $[\mathbf{A_c},\ \mathbf{B_c},\ \mathbf{C_c},\ \mathbf{D_c}]$ are the state-space matrices of the DT and CT loop filters respectively. MATLAB function $d2c$ does the DT to CT conversion with an NRZ pulse DAC, even with a singular matrix $(\mathbf{A_d} - \mathbf{I})$ in Eq. 5.67. The MATLAB code shown in Figure 5.50 gives the same $H(s)$ as Eq. 5.65.

```
<< Calculus`LaplaceTransform`

In[1]:= Rs = (1 - e^-s)/s;
        InverseLaplaceTransform[Rs, s, t];
        Hs = (b0 s^2 + b1 s + b2)/s^2;
        Gs = Hs × 1/s;
        gt = InverseLaplaceTransform[Gs, s, n]

Out[5]= b0 + b1 n + b2 n^2/2

        << DiscreteMath`ZTransform`

In[6]:= gt2 = 1;
        Fz = ZTransform[gt, n, z];
        Hzc = Cancel[Fz × (1 - z^-1)]
        Hz = (0.886 z - 0.614)/(z^2 - 2 z + 1);
        SolveAlways[Hzc == Hz, z]

Out[8]= 1/(2 (-1 + z)^2) (2 b0 - 2 b1 +
          b2 - 4 b0 z + 2 b1 z + b2 z + 2 b0 z^2)

Out[10]= {{b0 → 0., b1 → 0.75, b2 → 0.272}}
```

Figure 5.49. MATHEMATICA code for the DT loop filter to CT conversion with an NRZ DAC.

```
z=zpk('z');
Hz=(0.886*z-0.614)/(z^2-2*z+1);
Hz.ts=1;
Hs=d2c(Hz);
```

Figure 5.50. MATLAB code for the DT loop filter to CT conversion with an NRZ DAC.

5.7.2 CT SDM with RZ DAC Pulse

When an RZ DAC is employed for the CT SDM design, the transfer function along the loop becomes

$$\begin{aligned}\hat{G}(z) &= \mathcal{Z}\left[H(s)\frac{1-e^{-0.5s}}{s}\right] \\ &= \mathcal{Z}\left[\frac{H(s)}{s}\right] - \mathcal{Z}\left[\frac{H(s)e^{-0.5s}}{s}\right].\end{aligned} \tag{5.70}$$

Conventional z-transform cannot be applied for the second term in Eq. 5.70 because it is not valid for z-transform to represent any events occurring between two consecutive sampling instants. To solve this problem, so-called modified z-transform [56] is developed

for the conversion including variations inside a sampling period. By using modified z-transform, Eq. 5.70 can be rewritten as

$$\hat{G}(z) = \mathcal{Z}_{m_1}\left[\frac{H(s)}{s}\right] - \mathcal{Z}_{m_2}\left[\frac{H(s)}{s}\right], \tag{5.71}$$

where the subscripts $m_1 = 0$ and $m_2 = 0.5$ represent the pulse width inside a sampling period. Eq. 5.71 can be solved by using the residue theorem [57] as

$$\hat{G}(z) = \sum_{p_i} \text{Res}\left[\frac{H(s)}{s}\frac{e^{m_1 s}}{z - e^s}\right] - \sum_{p_i} \text{Res}\left[\frac{H(s)}{s}\frac{e^{m_2 s}}{z - e^s}\right], \tag{5.72}$$

where p_i are the poles of $H(s)/s$ and Res$[\cdot]$ is the residue at each pole.

As same as the conversion with an NRZ DAC, by comparing $\hat{G}(z)$ and $H(z)$, the loop filter of a CT SDM with an RZ DAC is then obtained.

[**Example**] For the same DT loop filter given by Eq. 5.61 and the same CT SDM topology illustrated in Figure 5.48, the equivalent DT transfer function of the CT LPSDM with an RZ DAC can be expressed as

$$\begin{aligned}\hat{G}(z) &= \sum_{p_i} \text{Res}\left[\frac{b_0 s^2 + b_1 s + b_2}{s^3}\frac{1}{z - e^s}\right]\Bigg|_{s=p_i} - \sum_{p_i} \text{Res}\left[\frac{b_0 s^2 + b_1 s + b_2}{s^3}\frac{e^{0.5s}}{z - e^s}\right]\Bigg|_{s=p_i} \\ &= \text{Res}\left[\frac{b_0 s^2 + b_1 s + b_2}{s^3}\frac{1}{z - e^s}\right]\Bigg|_{s=0} - \text{Res}\left[\frac{b_0 s^2 + b_1 s + b_2}{s^3}\frac{e^{0.5s}}{z - e^s}\right]\Bigg|_{s=0}. \end{aligned} \tag{5.73}$$

Since $H(s)/s$ only has a third-order pole, one residue calculation for each term in Eq. 5.73 is required. Once again, symbolic tools are used to calculate the residue. The MATHEMATICA code to solve Eq. 5.73 is presented in Figure 5.51, and the coefficients are found to be $[b_0,\, b_1,\, b_2] = [0,\, 1.364,\, 0.544]$. The CT loop function is then obtained as

$$H(s)_{RZ} = \frac{1.364s + 0.544}{s^2}. \qquad \square \tag{5.74}$$

The DT to CT conversion with an RZ feedback DAC also can be done in state-space. Schreier reveals that the difference between the CT counterpart with an NRZ and an RZ DACs is only the state-space matrix $\mathbf{B}$ by [58][47]

$$\mathbf{B_{cRZ}} = \left(e^{-\mathbf{A_c}} - e^{0.5\mathbf{A_c}}\right)^{-1}(\mathbf{A_d} - \mathbf{I})\mathbf{B_c}. \tag{5.75}$$

If the matrix $\left(e^{-\mathbf{A_c}} - e^{0.5\mathbf{A_c}}\right)$ is singular in Eq. 5.75, a little perturbance can be put onto $\mathbf{A_c}$ for the inverted matrix calculation [55]. The MATLAB code shown in Figure 5.52 gives the same CT loop filter as expressed in Eq. 5.74.

```
In[1]:= Hs = (b0 s^2 + b1 s + b2)/(a2 s^2 + a1 s + a0);
        a2 = 1;
        a0 = 0;
        a1 = 0;
        Gs = Hs × 1/s;
        Poles =
          Solve[s (a0 + a1 s + a2 s^2) == 0, s];
        m1 = 1;
        m2 = 0.5;
        Res11 = Residue[Gs e^(m1 s)/(z - e^s), {s, 0}];
        Res21 = Residue[Gs e^(m2 s)/(z - e^s), {s, 0}];
        Gz = Res11 - Res21
        Hz = (0.886 z - 0.614)/(z^2 - 2 z + 1);
        SolveAlways[Gz == Hz, z]
Out[13]= {{b1 → 1.364, b2 → 0.544}}
```

Figure 5.51. MATHEMATICA code for the DT loop filter to CT conversion with an RZ DAC.

```
z=zpk('z');
Hz=(0.886*z-0.614)/(z^2-2*z+1);
Hz.ts=1;
HsSSnrz=ss(Hz);
HsSSnrz=d2c(HzSSnrz);
HsSSrz=HsSSnrz;
HsSSnrz.a=[1 -0.5; 2 -1.0001];        % modify Ac to avoid singular matrix;
HsSSrz.b=inv(expm(HsSSnrz.a)-expm(0.5*HsSSnrz.a))*(HzSSnrz.a-eye(2))*HsSSnrz.b;
HsRZ=tf(HsSSrz);
```

Figure 5.52. MATLAB code for the DT loop filter to CT conversion with an RZ DAC.

The benefit of using an RZ DAC is that it is insensitive to the access loop delay. When the delayed RZ feedback pulse is inside the same sampling period as illustrated in Figure 5.53, the discrete to continuous conversion can be performed by a generalised formula in state-space as [47]

$$\mathbf{B_{cRZ}} = \left[e^{-\mathbf{A_c}(\mathbf{1}-\tau)} - e^{(0.5+\tau)\mathbf{A_c}}\right]^{-1} (\mathbf{A_d} - \mathbf{I})\mathbf{B_c}, \tag{5.76}$$

where τ is the delay.

For the NRZ DAC, any small delay extends the feedback pulse into the next sampling period, thus introduces ISI, as depicted in Figure 5.53. Therefore, the current feedback depends not only on the current symbol but also on the previous one. Using the modified z-transform method, it can be found that the access delay in a CT SDM with an NRZ feedback DAC increases the order of the DT equivalence by one [55], so that it is

not possible to compensate for the delay when converting the DT loop filter to the CT counterpart.

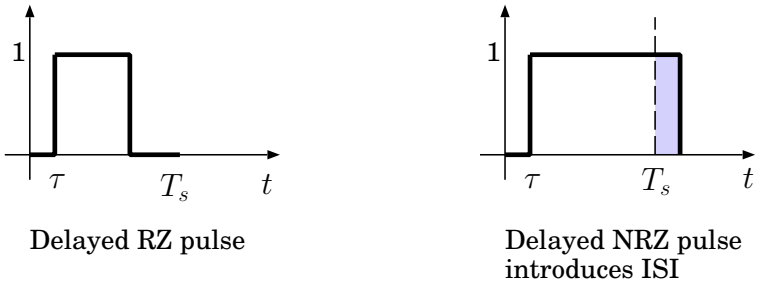


Figure 5.53. Delayed RZ and NRZ feedback pulses.

Although the RZ feedback pulse is insensitivity to the access delay, the switching speed of an RZ DAC is equivalent to double of that of an NRZ DAC, challenging the quantiser operating speed. If the quantiser is not fast enough to judge the input signal, a weak pulse is then presented at the quantiser output. The effect of weak pulses is the same as that of the clock jitter, directly whitenning the inband spectrum. The selection of the feedback DAC type should be considered with the circuit level analysis of the access loop delay and the achievable quantiser speed. In Chapter 6, the trade-off between the loop access delay and the DAC pulse type is further discussed.

5.7.3 Distributed feedback CT SDM

The designs of CT SDMs using the distributed feedback topology have been reported in [59][60]. A third-order CT LPSDM using the distributed feedback topology is illustrated in Figure 5.54. The distributed feedback paths break the loop filter, so that unlike the single loop CT SDM, there is no direct loop filter in a distributed feedback CT SDM. Therefore, the previous discussions of the DT loop filter to CT conversion is not available for the distributed feedback loop topology. This perhaps is the reason that none of [59] and [60] analysed the CT equivalent NTF. Without the control of the CT NTF, second-order CT SDMs might be the maximum achievable order presented in those publications.

The NTF of a distributed feedback CT SDM also can be obtained by converting the DT transfer function to the CT counterpart along each loop, if the zeros of the DT NTF are Butterworth type. For the third-order CT SDM illustrated in Figure 5.54, there are three feedback loops, of which the transfer functions $H_1(s)$, $H_2(s)$ and $H_3(s)$ can be

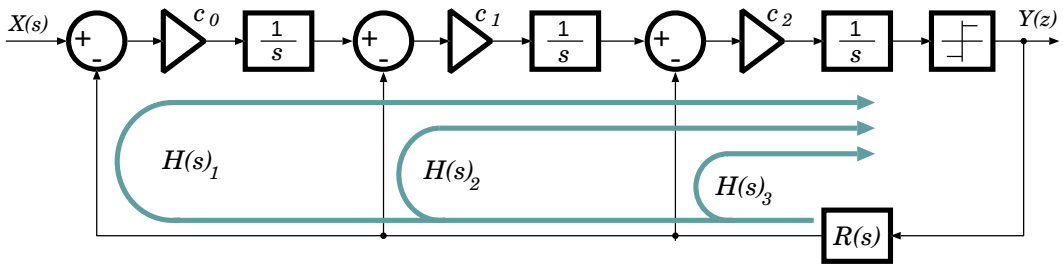


Figure 5.54. 3rd-order CT LPSDM using the distributed feedback topology.

written as

$$H_1(s) = c_0c_1c_2\frac{1}{s^3}R(s), \tag{5.77}$$

$$H_2(s) = c_1c_2\frac{1}{s^2}R(s), \tag{5.78}$$

$$H_3(s) = c_2\frac{1}{s}R(s), \tag{5.79}$$

where c_0, c_1, c_2 are the gain variables and $R(s)$ is the transfer function of the DAC. By applying z-transform to the three transfer functions, the total DT equivalent loop filter $\hat{G}(z)$ can be expressed as

$$\begin{aligned}\hat{G}(z) &= \mathcal{Z}[H_1(s)] + \mathcal{Z}[H_2(s)] + \mathcal{Z}[H_3(s)] \\ &= c_1c_2c_3\mathcal{Z}\left[\frac{1}{s^3}R(s)\right] + c_1c_2\mathcal{Z}\left[\frac{1}{s^2}R(s)\right] + c_2\mathcal{Z}\left[\frac{1}{s}R(s)\right].\end{aligned} \tag{5.80}$$

When the CT SDM is equivalent to a DT prototype, $\hat{G}(z)$ should be equal to the synthesised DT loop filter $H(z)$. With a chosen DAC pulse and solving $\hat{G}(z) = H(z)$ for the variables c_0, c_1, c_2 yields the desired equivalent CT SDM.

[**Example**] For a 3rd-order DT LPSDM the loop filter is synthesised as

$$H(z) = \frac{0.8114z^2 - 1.325z + 0.5606}{z^3 - 3z^2 + 3z - 1}. \tag{5.81}$$

When an NRZ DAC is employed, MATLAB function $c2d$ can be used for the s-domain to z-domain conversion in Eq. 5.80 and gives $\hat{G}(z)$ as

$$\hat{G}(z) = c_0c_1c_2\frac{0.1667z^2 + 0.6667z + 0.1667}{(z-1)^3} + c_1c_2\frac{0.5z + 0.5}{(z-1)^2} + c_2\frac{1}{z-1}. \tag{5.82}$$

Comparing Eq. 5.81 to Eq. 5.82 and solving for the coefficients c_i gives

$$[c_0,\ c_1,\ c_2]_{NRZ} = [0.1874,\ 0.3698,\ 0.6782]. \tag{5.83}$$

When $R(s)$ is an RZ pulse DAC, Eq. 5.80 can be converted in state-space by modifying the state matrix $\mathbf{B}_d$ as [47]

$$\mathbf{B}_d = \mathbf{A}_c^{-1}\left(e^{\mathbf{A}_c} - e^{0.5\mathbf{A}_c}\right)\mathbf{B}_c. \tag{5.84}$$

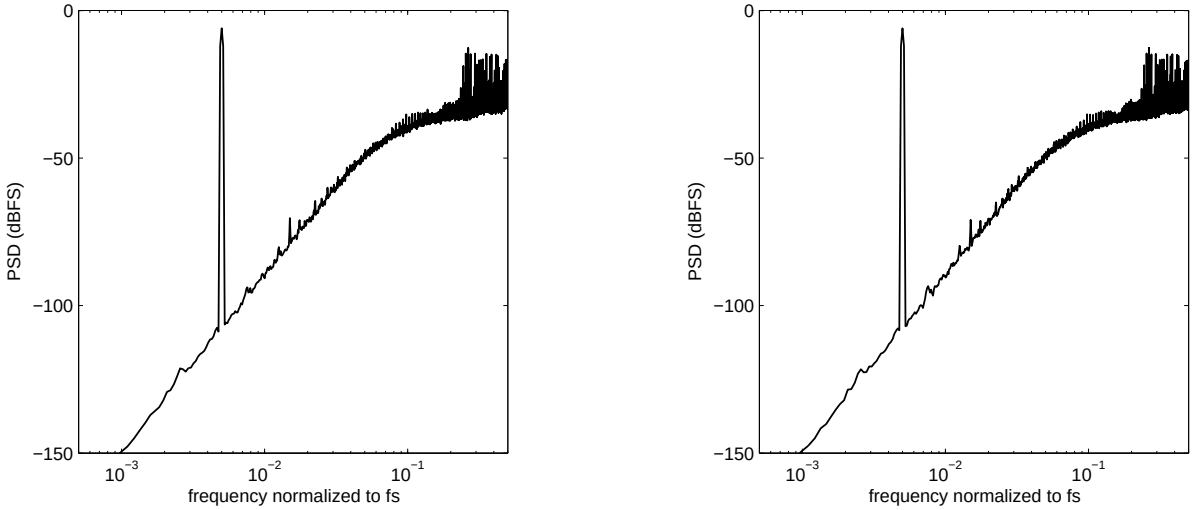
Once again, if $\mathbf{A}_c^{-1}$ is singular, a small error can be added on for the inverted matrix calculation. By using the modified matrix $\mathbf{B}_d$, the equivalent DT transfer function $\hat{G}(s)$ with an RZ DAC is derived as

$$\hat{G}(s) = c_0c_1c_2\frac{0.1458z^2 + 0.3333z + 0.0208}{(z-1)^3} + c_1c_2\frac{0.375z + 0.125}{(z-1)^2} + c_2\frac{0.5}{z-1}. \tag{5.85}$$

The coefficients c_i thereby are calculated as

$$[c_0,\ c_1,\ c_2]_{RZ} = [0.1967,\ 0.3866,\ 1.2368]. \tag{5.86}$$

The synthesised third-order CT LPSDM can be evaluated using SIMULINK. Figure 5.55 shows the PSD plots of the modulator with an NRZ and an RZ DACs. Both of the graphics present the same spectrums since they are all equivalent to the same DT loop filter of Eq. 5.81.□



(a) (b)

Figure 5.55. Simulated PSDs of the 3rd-order LPSDM using the distributed feedback topology with an (a) NRZ DAC and (b) RZ DAC.

5.8 Summary

In this chapter a review of the fundamentals of SDM is conducted. From the review it is identified that none of the stability criteria for the NTF are adequate for the NTF synthesis, hence simulation based approaches based on state-space and Simulink are adopted. However, to improve the simulation speed, the SDM transfer function is evaluated using state-space, and then Simulink is used as a bridge of mapping the transfer function to the circuit building blocks. This approach is demonstrated through the design of a DT VCF BPSDM, and a CT LPSDM as discussed in Chapter 6.

Another contribution of this research is the development of a new resonator architecture that allows the design of DT VCF BPSDMs. In contrast to the common approach in the literature that uses a continuous filter, which results in limiting the controllability of the NTF and its order. The presented approach enables a well controlled NTF that covers all the tuning range and can have up to 4th or higher orders. This design approach is validated through measurements from fabricated structures of a 4th-order switched-capacitor VCF BPSDM using the AMI 1.5 µm CMOS process.

In addition, a detailed analysis to the design of distributed feedback CT SDMs was presented. The NTF of a CT SDM can be synthesised with multiple feedbacks in contrast what is commonly used in the literature where such topology often used for DT SDMs.

A wide variety of SDM topologies are available for oversampling ADC designers. The selection of a proper SDM topology is based on the performance criteria, circuit complexity, oversampling ratio and power consumption, etc. In the next chapter, the circuit level design of a 1 GHz 2nd-order CT LPSDM is presented.

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Chapter 6

Design of a 1 GHz Lowpass Sigma-Delta Modulator

6.1 Introduction

To meet the challenge of large bandwidth, high order and multi-bit SDMs have been reported in the literature [61][62][63][64] . High order SDMs are more effective in noise shaping, whereas multi-bits SDMs have better analog-to-digital conversion resolution. Therefore to maintain the same performance, a lower OSR can be used to avoid the challenge of the high-speed analog circuit design. Also, the OTA gain bandwidth is not a critical issue in the low speed region, so more choices are available for the SDM loop filter implementation. On the other hand, high order SDMs have more complicated NTF and may suffer from instability. Multi-bit SDMs require multi-bit DACs for the analog feedback and are more prone to mismatch between circuit components. In addition, due to the low OSR, a high order anti-aliasing analog filter is required before a DT SDM, which also complicates the overall system design.

Another approach to meeting the challenge of large bandwidth is to employ high speed low order CT SDM ADCs. The low efficiency of the noise shaping due to a simple NTF is compensated for by a large oversampling frequency. Sophisticated InP processes with very high f_T transistors are used in the literature to design SDMs operating over 1 GHz [59][60]. Transistors in these technologies consume large current, which is a major

drawback for mobile applications. In addition, InP fabrication process is not compatible with CMOS process and hence limits the integrations for SOC systems.

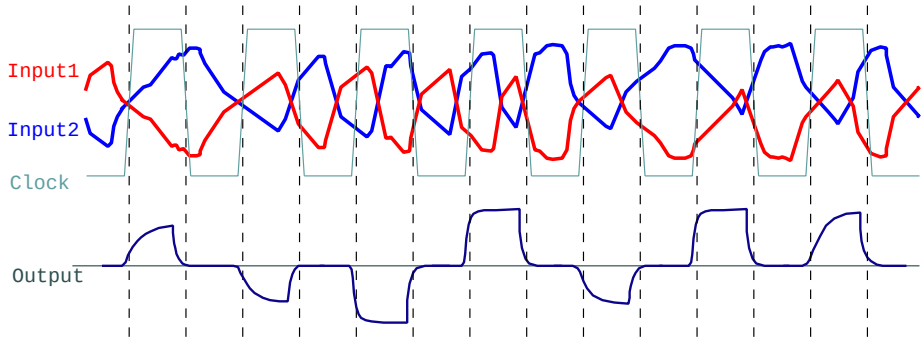
In this chapter, the design of a 1 GHz CT LPSDM using the TSMC 0.18 µm CMOS process is presented. The system level analysis is first introduced followed by the design of circuit building blocks, including the integrator, loop filter and the high-speed quantiser. Finally the simulation results of the whole modulator and the layout are illustrated.

6.2 System Level Analysis and NTF Synthesis

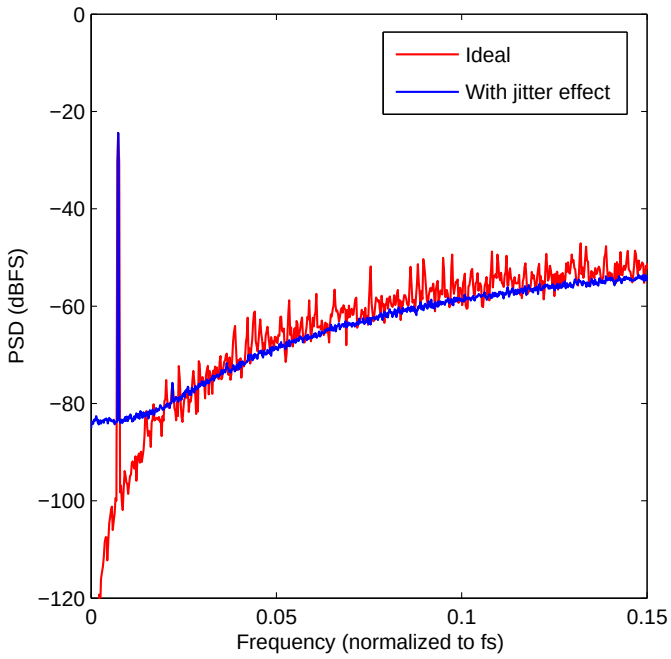
As discussed in Chapter 5, a CT SDM is a combined z and s-domain system, therefore a direct synthesis of its NTF is difficult. The design of a CT SDM loop filter is achieved by synthesising a DT loop filter, then convert it to the CT counterpart associated with the feedback DAC pulse shape.

An RZ pulsed DAC is insensitive to the access loop delay because the delayed pulse is still inside the same sampling period, and hence can be compensated for by adjusting the loop filter transfer function according to Eq. 5.76. On the other hand, an RZ DAC requires an RZ comparator with an effective frequency equivalent to double that of an NRZ comparator. For a 1 GHz SDM, 2 GHz pulses are presented at the RZ comparator outputs, challenging the comparator design using a CMOS process. When the quantiser clock speed is approaching the comparator speed limit, weak pulses appear when the two input signals have small difference at the comparison time, as shown in Figure 6.1(a). The weak pulses introduce energy uncertainty in the feedback pulses, which has the same effect of the clock jitter, whitening the spectrum in the signal band, as shown in Figure 6.1(b). Since the inband noise power is crucial for the SNR, the whitened spectrum in the signal band has a strong impact on the SDM resolution.

When an NRZ DAC pulse is applied, the quantiser speed criteria is relaxed. However, any loop access delay shifts the DAC pulse to the next sampling period, increasing the loop filter order. As illustrated in Figure 6.2, assuming the delay is τ, then the delayed NRZ pulse can be treated as a linear combination of a DAC pulse from τ to 1 and a delayed DAC pulse from 0 to τ [55]. Then the equivalent transfer function including the



(a)



(b)

Figure 6.1. (a) Weak output pulses due to the comparator speed limitation; (b) whitened PSD in the signal band due to the jitter effect.

loop filter and the DAC is given by

$$\begin{aligned} G(s) &= H(s)[R(s)_1 + R(s)_2] \\ &= H(s)\frac{e^{-\tau s} - e^{-s}}{s} + H(s)e^{-s}\frac{1 - e^{-\tau s}}{s}, \end{aligned} \tag{6.1}$$

where $H(s)$ is the CT loop filter and $R(s)_1$, $R(s)_2$ are the two DAC transfer functions. The DT counterpart of $G(s)$ is then given by the z-transform as

$$\begin{aligned}\hat{G}(z) &= \mathcal{Z}[G(s)] \\ &= \mathcal{Z}_m\left[H(s)\frac{e^{-\tau s}-e^{-s}}{s}\right] + z^{-1}\mathcal{Z}_m\left[H(s)\frac{1-e^{-\tau s}}{s}\right],\end{aligned} \tag{6.2}$$

which can be solved by the residue theorem of Eq. 5.72.

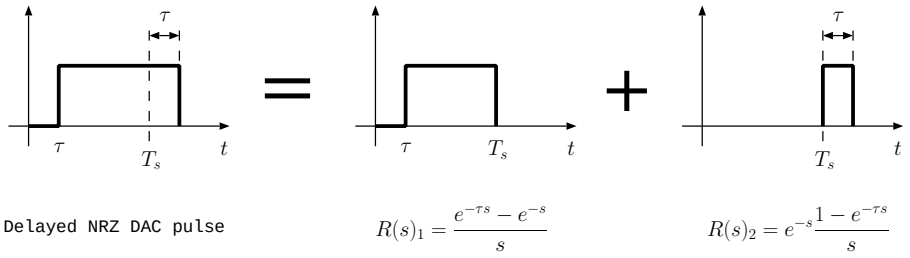


Figure 6.2. Delayed NRZ DAC pulse as a linear combination.

Making use of the CT loop filter shown in Eq. 5.65 as an example, the MATHEMATICA code illustrated in Figure 6.3 converts the CT loop filter to the DT counterpart with a delayed NRZ DAC as

$$H(z) = \frac{(-0.886+1.022\tau-0.136\tau^2)z^2+(0.614-1.772\tau+0.272\tau^2)z+(0.75\tau+0.136\tau^2)}{z(z-1)^2}. \tag{6.3}$$

As a verification, for $\tau = 0$, Eq. 6.3 returns to the non-delayed loop filter given by Eq. 5.61. Applying the quantiser linear model, the loop filter $H(z)$ is transferred into the NTF as

$$NTF(z) = \frac{z(z-1)^2}{z^3-(2.886-1.022\tau+0.136\tau^2)z^2+(1.614-1.772\tau+0.272\tau^2)z+(0.75\tau+0.136\tau^2)}. \tag{6.4}$$

Figure 6.4 presents the Pole-Zero plot and the magnitude responses of Eq. 6.4. The delayed NRZ DAC increases the order of the NTF by introducing an extra zero at the origin and an extra real pole, as shown in Figure 6.4(a). The zero at the origin does not affect the NTF magnitude response, however the real pole and the displacement of the other two poles make a sharper peak on the magnitude of the NTF when increasing the delay, as illustrated in Figure 6.4(b). This peak pushes the quantisation noise power towards the low frequency region, hence increases the inband noise power.

The simulated PSDs of Eq. 6.4 with different delays are shown in Figure 6.5. As predicted, the noise PSD also presents a peak towards the signal band, thereby reducing

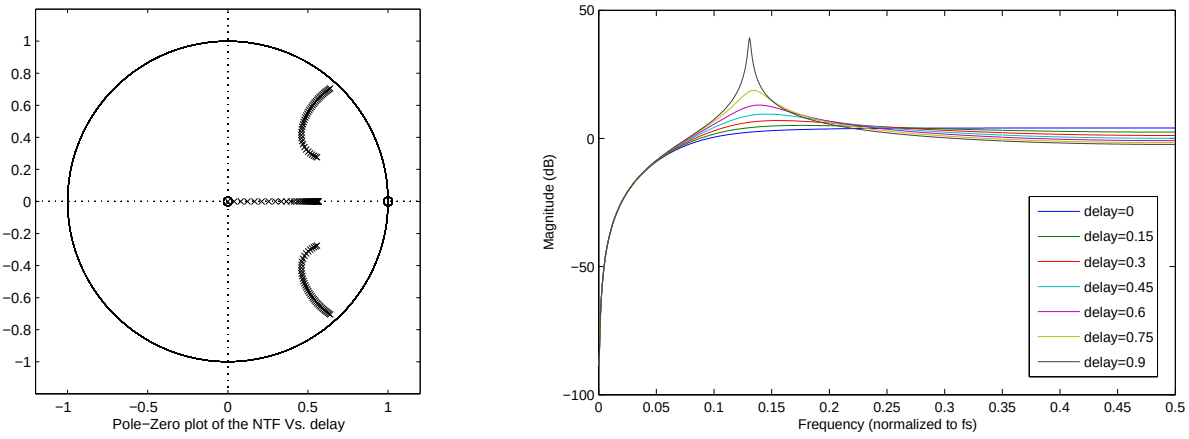
```
In[1]:= Hs = (b0 s^2 + b1 s + b2) / (a2 s^2 + a1 s + a0);
        a2 = 1;
        a0 = 0;
        a1 = 0;

        b2 = 0.272;
        b1 = 0.75;
        b0 = 0;


        Gs = Hs × 1/s;
        Gsd = Gs × e^-s;
        Poles =
          Solve[s (a0 + a1 s + a2 s^2) == 0, s];
        τd = τd;
        tH = 1;
        m1 = 1 - τd;
        m2 = 1 - 1;
        md1 = 1;
        md2 = 1 - τd;
        Res11 =
          Residue[Gs e^(m1 s)/(z - e^s), {s, 0}];

        Res21 = Residue[Gs e^(m2 s)/(z - e^s), {s, 0}];

        Res1d = Residue[Gs e^(md1 s)/(z - e^s), {s, 0}];

        Res2d = Residue[Gs e^(md2 s)/(z - e^s), {s, 0}];

        Gtmp = Simplify[Res11 - Res21];
        Gtmpd = z^-1 Simplify[Res1d - Res2d];
        Gz = Simplify[Cancel[Gtmp + Gtmpd]];
```

Figure 6.3. MATHEMATICA code for the CT loop filter to DT conversion with a delayed NRZ DAC.

the SNR. However, the delayed NRZ DAC does not directly whiten the inband noise spectrum. For a narrow band, or large OSR application, comparing Figure 6.1(b) and Figure 6.5, the SNR degradation due to the delayed NRZ DAC pulse is much less than that of the weak pulses due to the quantiser speed limit. As a conclusion, in this 1 GHz LPSDM design, the NRZ DAC pulse is chosen.

The DT loop filter of Eq. 5.61 is selected for the second-order LPSDM design. When a delayed quantiser is employed, the extra z^{-1} in the quantiser has to be compensated for in the loop filter. This can be achieved by multiplying the loop filter transfer function by z, resulting in the final DT loop filter transfer function as

$$H(z)_{Delayed} = z \times H(z) = \frac{0.886z^2 - 0.614z}{z^2 - 2z + 1}. \tag{6.5}$$



(a) (b)

Figure 6.4. (a) Pole-Zero plot of the NTF Vs. the delay; (b) magnitude response of the NTF with different delays

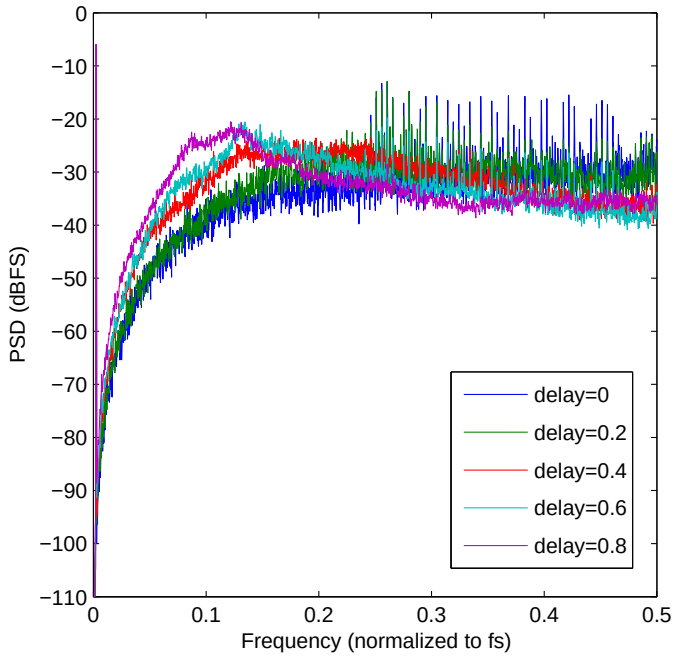


Figure 6.5. Output spectrums of the 2nd-order LPSDM of Eq. 6.3 with different delays.

This DT loop filter is then converted into the CT counterpart with an NRZ DAC as

$$\begin{aligned} H(s)_{Delayed} &= d2c[H(z)_{Delayed}] \\ &= \frac{0.886s^2 + 1.022s + 0.272}{s^2}. \end{aligned} \tag{6.6}$$

The CT loop transfer function can be evaluated using SIMULINK as shown in Figure 6.6(a). The system level simulation of the ideal CT LPSDM gives a SNR of 80 dB and a dynamic range of 85 dB with an OSR of 100. Non-idealities, such as circuit noise, clock jitter and quantiser hysteresis etc. can be analysed using this SIMULINK model [65].

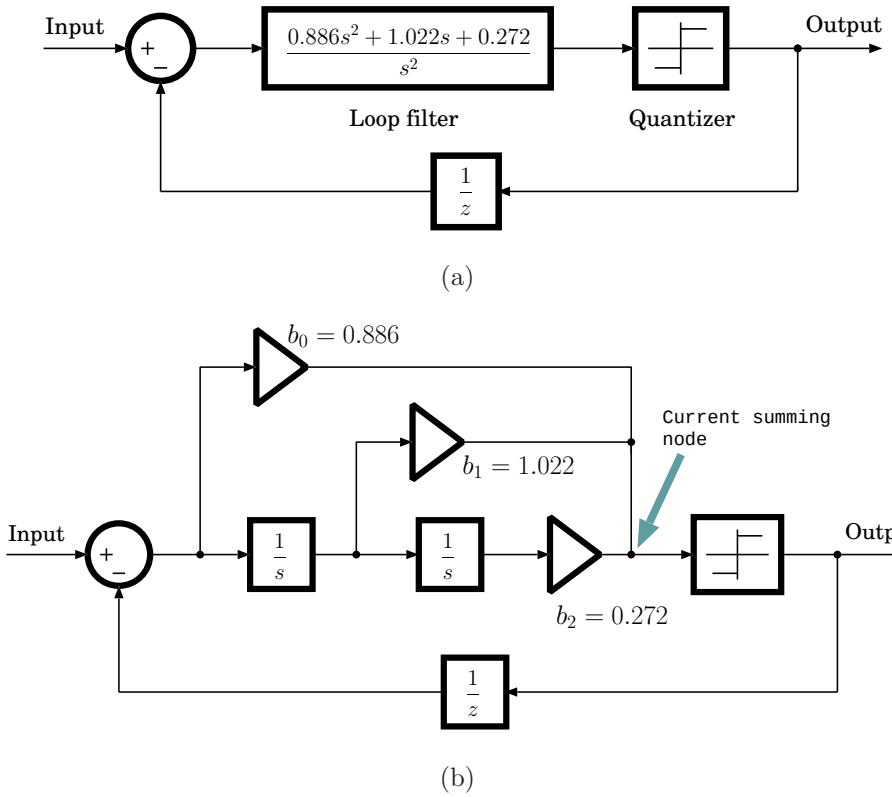


Figure 6.6. SIMULINK models of the 2nd-order CT LPSDM with a delayed NTF. (a) Transfer function model and (b) topology realisation.

The CT loop transfer function can be implemented using continuous-time integrator elements, as shown in Figure 6.6(b). Working out the coefficients to realise Eq. 6.6 gives $[b_0, b_1, b_2] = [0.886, 1.022, 0.272]$. These coefficients can be scaled to an achievable range for the circuit design using linearised transconductor techniques.

6.3 Loop Filter Design

The circuit realisation of the CT loop filter using the $G_m - C$ technique in differential mode is illustrated in Figure 6.7. The G_m value can be calculated by transforming the variable s to s/f_s, where $f_s = 1$ GHz is the sampling frequency of the quantiser. The integrator capacitor C_{int} was chosen first. For $C_{int} = 0.5$ pF, the integrator G_m is calculated as 0.5 mS and the coefficients $[b_0, b_1, b_2]$ as [0.886, 1.022, 0.272] mS. All of these values are appropriate for the circuit integration using the chosen CMOS process.

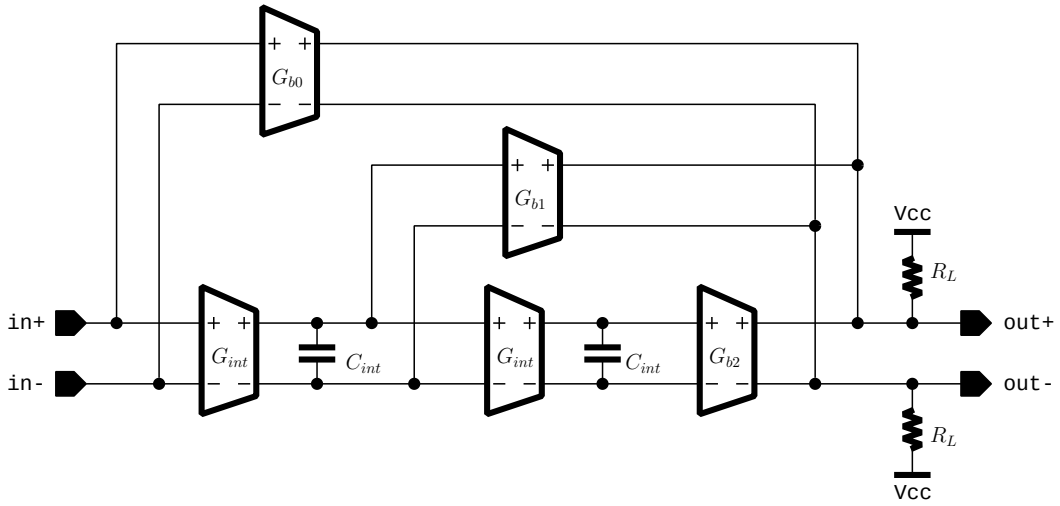


Figure 6.7. Circuit realisation of the CT loop filter using the $G_m - C$ technique.

The $G_m - C$ integrator is the most critical building block for the loop filter design, because the integrator DC gain decides the inband noise shaping efficiency, and its frequency response realises the loop filter transfer function. An ideal $G_m - C$ integrator is shown in Figure 6.8(a). The input voltage signal is converted into a current signal by the transconductor, resulting in a voltage across the capacitor C_{int}. All the transconductor output current drives the capacitor in this ideal model, yielding the integrator transfer function as $g_m/(sC_{int})$ that has an infinite DC gain.

However in circuit design, a load is always required to bias the G_m and hence causes current leakage via the load, as illustrated in Figure 6.8(b). Such an integrator, sometimes referred to as a lossy integrator, has reduced gain especially at DC, whitening the noise spectrum in the signal band. This issue directs the design focus toward increasing the output resistance of the transconductor loads. For example, active loads with cascaded transistors can be used for this purpose [66] as shown in Figure 6.8(c). However in

that circuit configuration, a CMFB circuitry is necessary to stabilise the common-mode output, complicating the analog circuit design at high frequencies. Also the large parasitic capacitance at the output nodes limits the gain bandwidth of the integrator. In this design if the parasitic capacitance at the output nodes is larger than 0.5 pF, then it is not possible to realise the integrator transfer function for the loop filter when using the same transconductor.

Another approach to have a large integrator DC gain is to compensate for the current using a negative transconductance as illustrated in Figure. 6.8(d), which is often used in an LC resonator circuit to boost the Q-factor. The negative G_m compensation technique also can be interpreted as that if the equivalent resistance of G_{qb} is equal to R_L but with the opposite polarity, they cancel each other, and the integrator turns into Figure 6.8(a). The benefit of using the negative G_m compensation technique is that a lossy integrator with resistive loads can be used, simplifying the circuit design at high frequencies. Also the small parasitic capacitance at the output nodes makes it possible to realise the CT loop filter of Eq. 6.6.

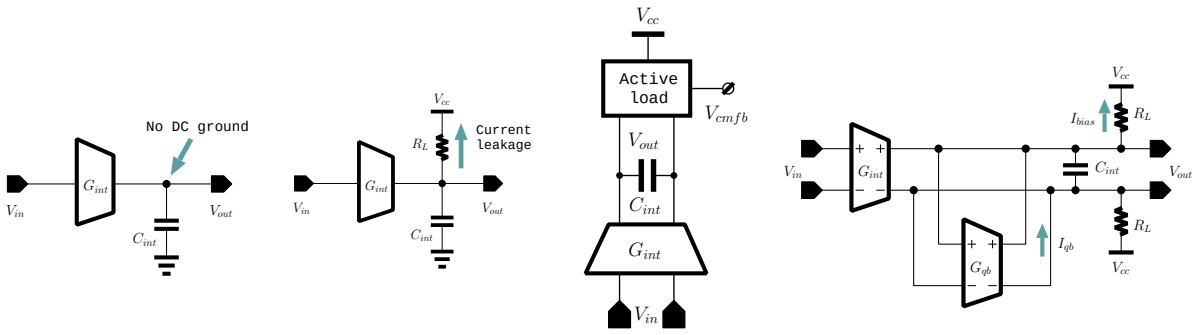


Figure 6.8. Continuous-time integrator modelling. (a) Ideal, (b) lossy due to the resistance bias, (c) with active loads, and (d) with resistance loads and negative transconductance compensation.

The integrator shown in Figure 6.8(d) can be implemented using cross-coupled transconductance elements labelled G_{int} and G_{qb} respectively, as illustrated in Figure 6.9. The summed current signals from the three paths are converted into voltage signals by the resistive loads R_L. Since there is no DC cancelling technique for the current summation, all the DC bias current is summed too. That is the reason for choosing 3.3 V MOSFETs for the loop filter design to have large voltage headrooms.

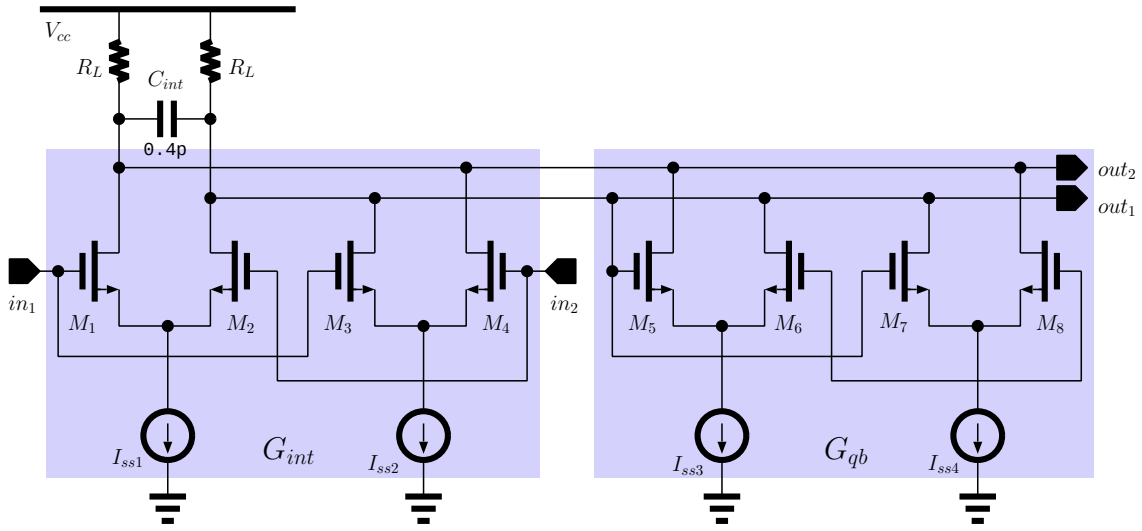


Figure 6.9. Integrator circuit realisation of Figure 6.8(d).

When the odd order non-linear terms of the transconductance of the two differential pairs M_1, M_2 and M_3, M_4 are the same, they can be eliminated by cross coupling the two differential pairs at a cost of reducing the fundamental transconductance term. Using the MOSFET square law, the differential pair output current can be presented in MaClaurin Series as [67]

$$I_o = \sqrt{2I_{ss}K}V_{id} + 0 - \frac{1}{2\sqrt{2}}\frac{K^{3/2}}{\sqrt{I_{ss}}}V_{id}^3 + 0 - \cdots, \tag{6.7}$$

where V_{id} is the differential input signal, K is equal to $\mu C_{ox}W/(2L)$, and I_{ss} is the tail current. The even order distortion is vanished due to the differential topology. When the third-order product of the two differential pairs are identical, we have

$$\left(\frac{K_{3,4}}{K_{1,2}}\right)^3 = \frac{I_{ss2}}{I_{ss1}}. \tag{6.8}$$

Assuming I_{ss1}=$2I_{ss2}$ and $L_{1,2} = L_{3,4}$, the third-order product cancellation happens when $W_{1,2}$=$1.26W_{3,4}$. In the submicron regime, the square law is no longer accurate because of the high electrical field in a short MOSFET channel. SPICE simulations show that a larger transistor width ratio, between 1.5 and 1.6, is required to compensate for the short channel effects, in contrast to 1.26 based on the square law model. The load resistors are chosen to have a 1.9 V DC output for the next stage circuit. The integrator transconductance is designed as 0.5 mS that drives a 0.4 pF capacitor load. The extra 0.1 pF is contributed by the total parasitic capacitance at the output nodes.

The integrator transconductance G_{int} versus V_{id} plot is shown in Figure 6.10, as well as the scaled voltage histograms at the two integrator input nodes. The direct observation shows that the constant transconductance range is much larger than the input signal variation range, hence good linearity is obtained.

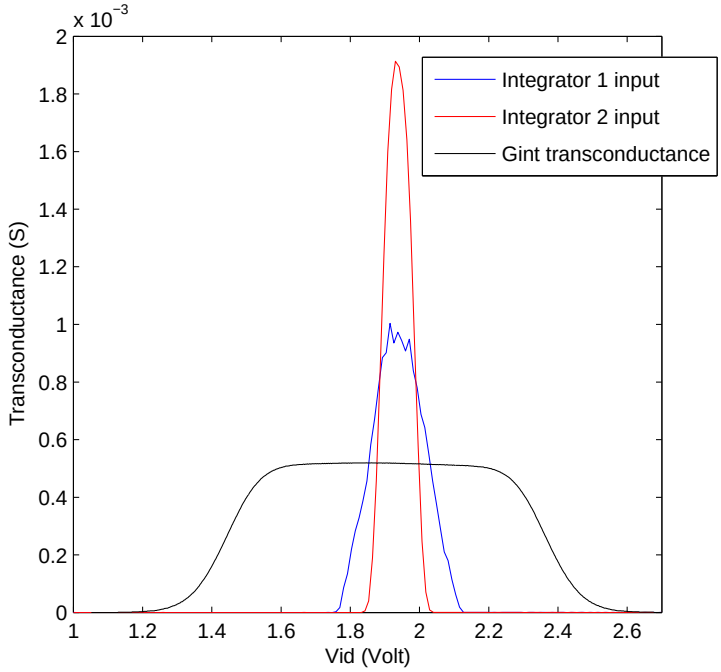


Figure 6.10. Simulated G_{int} transconductance and scaled input voltage histograms of the two integrators.

Because of the small output resistance, the lossy integrator has very poor gain at DC. A negative transconductor is connected at the output nodes to cancel the resistor loads, and thereby boost the DC gain. The design of the negative G_m can be achieved by first using a macro VCCS model to evaluate the gain boost and then implement it into a circuit equivalent. Figure 6.11 shows the gain boost processed by the negative G_m element. Under the perfect negative G_m tuning, the integrator DC gain can be over 85 dB and the frequency response is very close to the ideal one, so that the integrator transfer function is realised.

The coefficients $b_0 \sim b_2$ can also be realised using cross-coupled transconductors. The simulated frequency response of the CT loop filter of Eq. 6.6 is shown in Figure 6.12, as well as the ideal curve calculated using MATLAB. Since the transfer function of the integrator and the gain coefficients are accurately controlled, the circuit simulation and

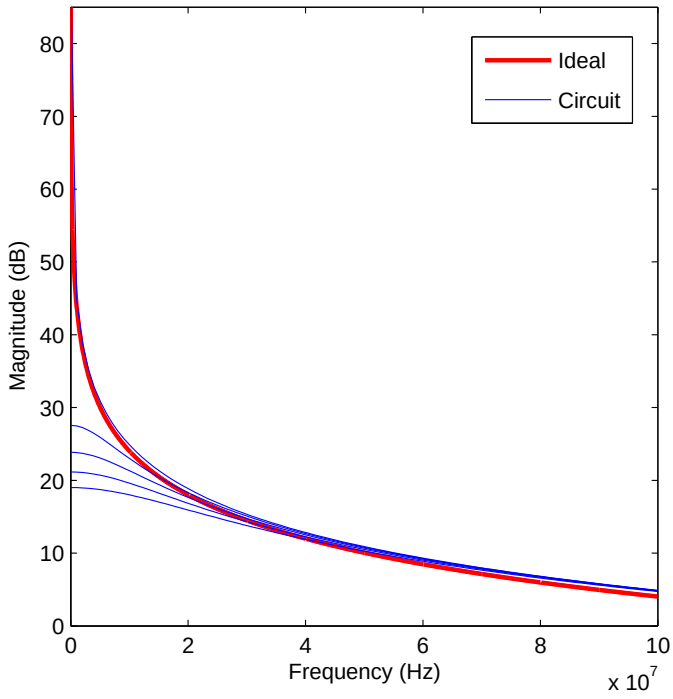


Figure 6.11. Integrator gain boost by the negative transconductance tuning.

the ideal frequency responses of the CT loop filter are almost identical. Therefore the SDM stability and the noise shaping quality are guaranteed.

6.4 High Speed Quantiser Design

The single-bit quantiser comprises an input buffer and 3 stages of a master-slave clocked comparator as shown in Figure 6.13. In order to achieve high speed operation, 0.18µm MOSFETs with 1.8 V supply voltage are used.

The input buffer isolates the clock kick-back noise from the clocked quantiser to the CT loop filter via the parasitic gate capacitance of M_1, M_2 and M_3, also offers a 6 dB voltage gain. Although a larger gain will alleviate the sensitivity of the subsequent comparator, the coherent larger delay will distort the NTF, since the CT SDM with an NRZ feedback DAC is sensitive to the access loop delay.

The low voltage master-slave comparator is formed by a differential pair and an RSA connected as the NRZ mode. The difference between the low voltage configuration and a conventional SCL master-slave comparator is that two current sources are required

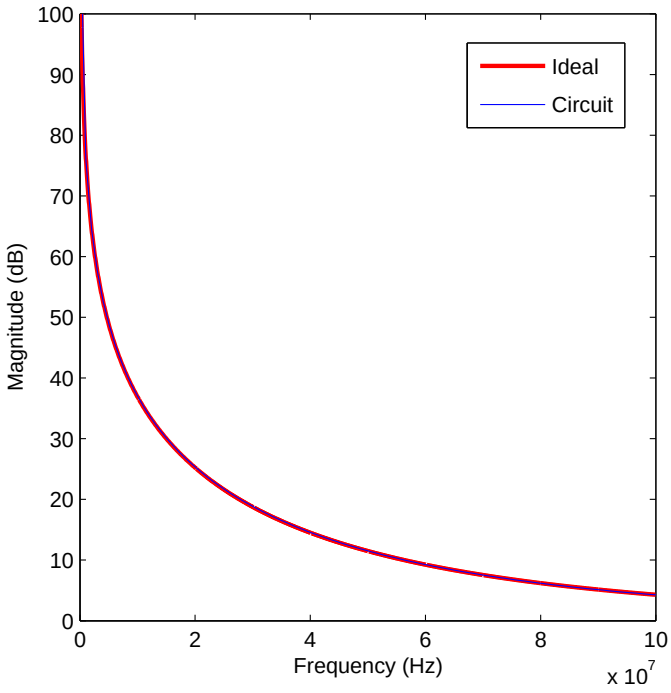


Figure 6.12. Frequency response of the CT loop filter.

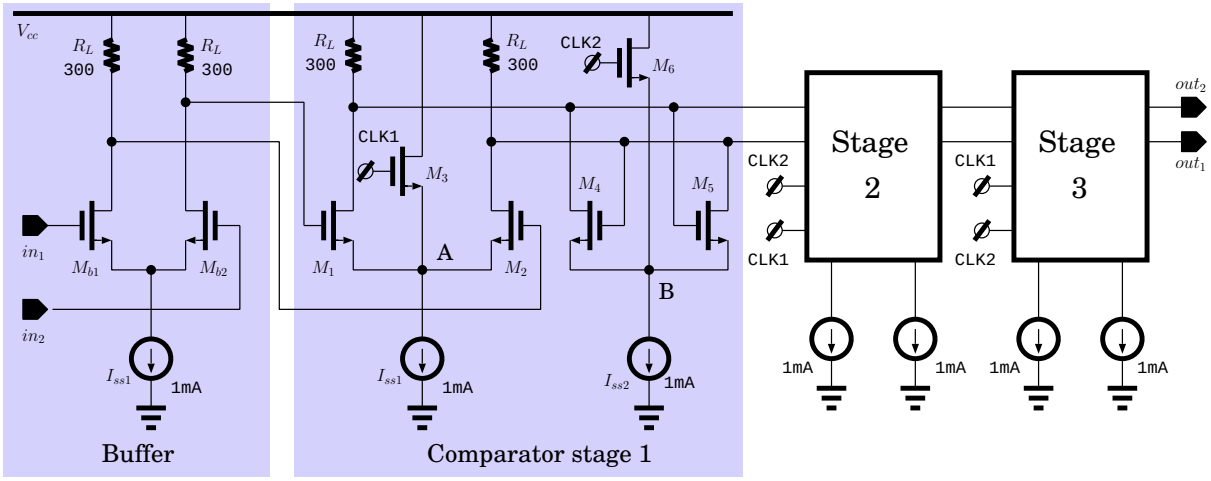


Figure 6.13. Schematic of the delayed quantiser.

for both the differential pair and the RSA, whereas in an SCL circuit only one current source steers between the differential pair and the RSA. So that the power consumption is doubled, however stacked transistors are avoided for low voltage applications.

CLK1 and CLK2 are the two phase clock inputs. When CLK1 is at high level V_{clkH}, M_3 shunts all of the tail current and boosts the voltage at node A, switching off the input differential pair. When CLK1 is at low level V_{clkL}, M_3 is switched off and enables

the differential pair for the input signal tracking. The same process occurs in the RSA, resulting in the regeneration of the output when CLK2 is low. The input DC level of both the differential pair and the RSA are biased at 1.65 V. The voltage swing of CLK1 and CLK2 should meet the boundary condition given by

$$\begin{aligned} V_{clkL} &< V_{g1} - \sqrt{\frac{I_{ss}}{2K_1}}; \\ V_{clkH} &> V_{g1} + \sqrt{\frac{I_{ss}}{K_3}}, \end{aligned} \tag{6.9}$$

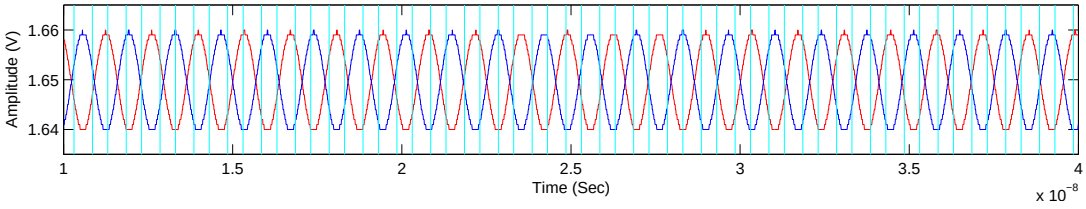
where $V_{g1} = 1.65$ V is the gate voltage of M_1, $I_{ss} = 1$ mA is the tail current, $K_1 = \mu_0 C_{ox} W_1/(2L_1)$ and $K_3 = \mu_0 C_{ox} W_3/(2L_3)$. The clock swing can be reduced to minimise the clock kick-back noise by increasing K_1 and K_3.

In order to improve the comparator recovery time, small resistor loads of 300 ohm are used for the differential pair and the RSA. The resistors set the output voltage swing to 0.3 V (1.65±0.15V) with a 1 mA tail current. Small resistors reduce the comparator gain, hence less sensitivity. To improve the sensitivity of the comparator while maintaining high speed operation, a three-stage comparator is applied. For each stage, the gain is comparatively small to favour the speed; the total comparator gain is the summation of the three stages together in decibel.

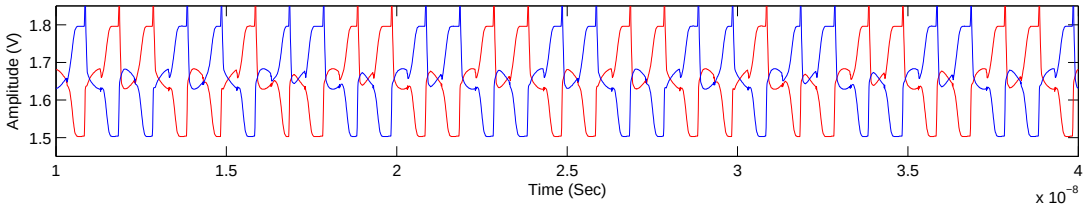
The simulated results of the comparator output at each stage are shown in Figure 6.14 with a 1 GHz differential clock and a 10 mV differential sinusoidal input. After three amplification stages and the buffer, the final output is a very good pulse waveform. The three-stage comparator with small resistor loads successfully solve the trade-off between the speed and sensitivity, however introduces one unit clock delay. This is the reason that a delayed NTF is synthesised.

6.5 Modulator Simulations and Layout

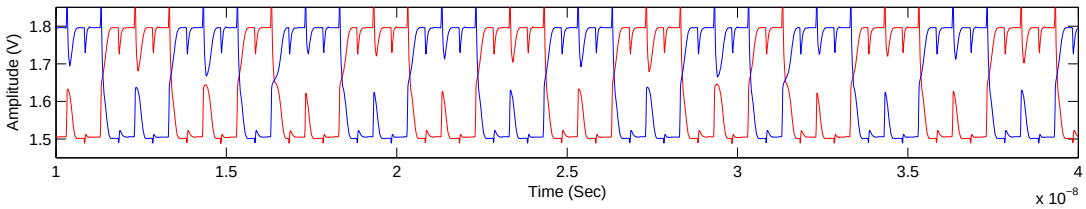
The overall circuit diagram of the CT LPSDM is shown in Figure 6.15. The feedback transconductor G_{fb} and input transconductor G_{in} set the input voltage range to 0.2 V, which is inside the linear range of the transconductors. To simulate the modulator, a differential sinusoidal signal is fed into the modulator and the output is then fed into MATLAB for spectrum analysis. In order to avoid the spectrum splatter, the input



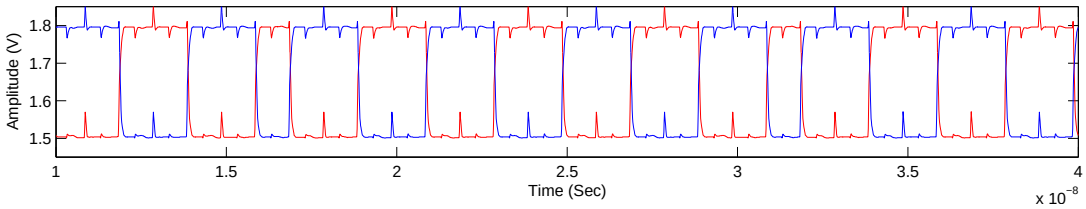
(a) Input signals and the clock



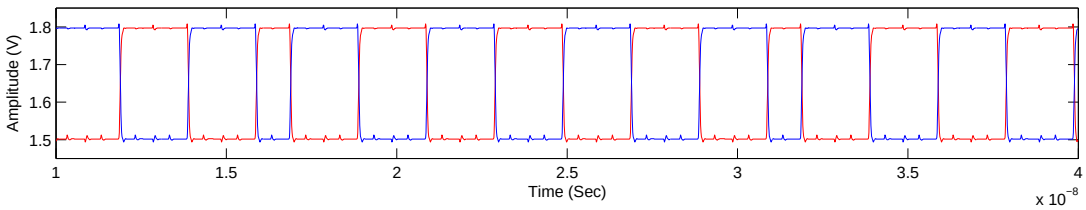
(b) Stage 1 output



(c) Stage 2 output



(d) Stage 3 output



(e) Buffered output

Figure 6.14. quantiser output at each stage with a ± 10 mV differential sinusoidal input.

sinusoidal frequency should be equal to N/t_{step}, where N is the data sequence length and t_{step} is the SPICE transient simulation time step. This is because the real sampling period of the simulated data stream is the SPICE transient simulation step instead of the sampling period of the quantiser in the circuit. The output data stream is Hann windowed before the Fourier-Transform to avoid the spectrum leakage.

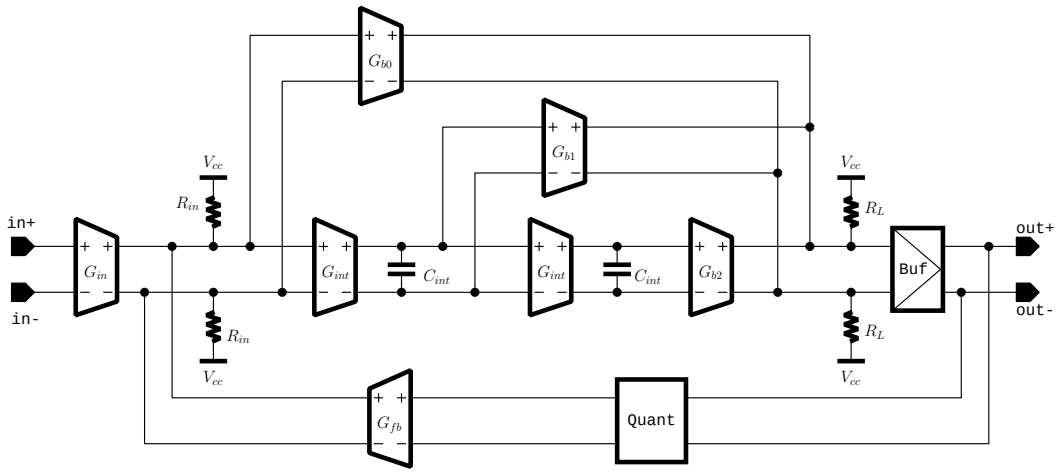


Figure 6.15. Circuit diagram of the 2nd-order CT LPSDM.

Figure 6.16 presents the PSD of the circuit level simulation of the second-order CT LPSDM. The input signal is a 3 MHz differential sinusoid with an amplitude of 0.15 V. The deep notch at DC is a result of the high DC gain of the integrators. The transfer function of the loop filter is accurately controlled by the linearised transconductors, so that a graceful noise shaping is obtained.

The SNR can be calculated by the signal power at 3 MHz divided by the total inband noise power. The modulator gives an SNR of 71 dB for a 5 MHz bandwidth and 62 dB for a 9 MHz bandwidth.

The layout of the stand-alone chip for the test purpose is shown in Figure 6.17(a). The clock buffer and the quantiser are isolated by double guard rings to reduce the substrate coupling. The size of the modulator core is about 500 µm×600 µm, as shown in Figure 6.17(b). The whole chip drains 16 mA from the 3.3 V supply voltage and 15 mA from the 1.8 V supply voltage, dissipating 80 mW power.

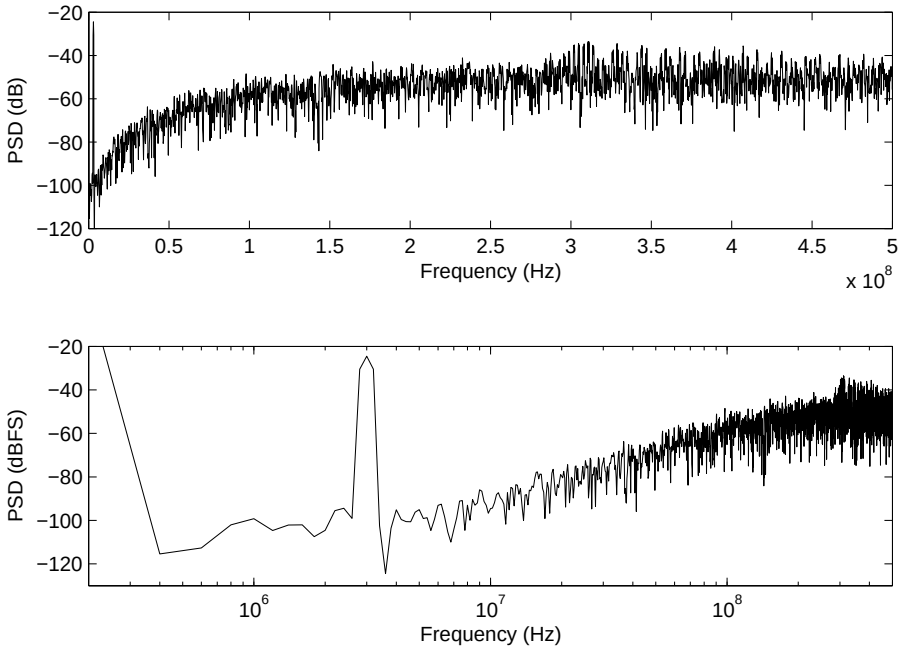
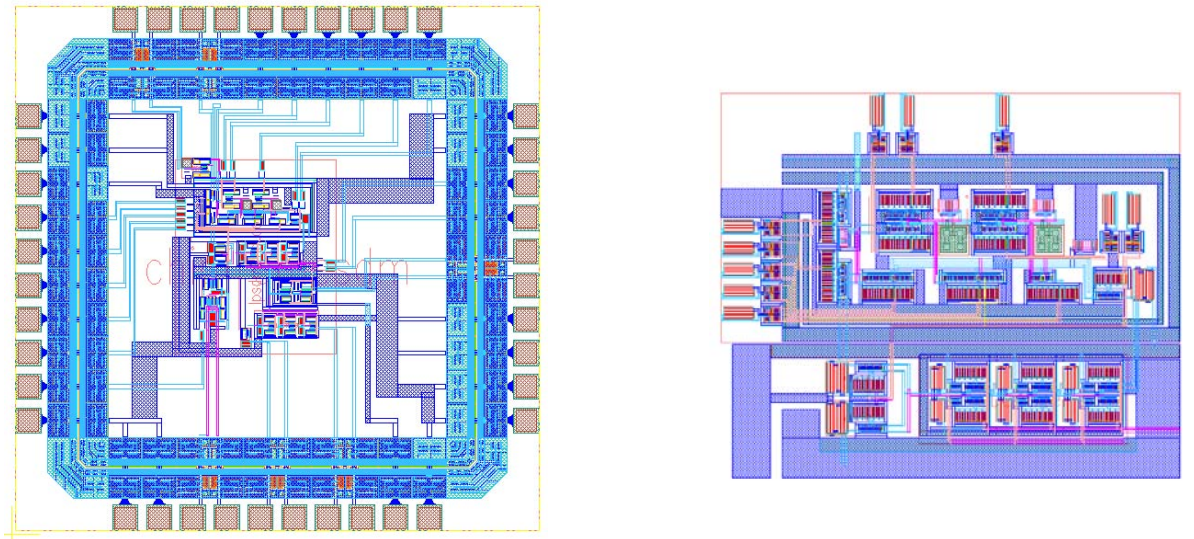


Figure 6.16. Transistor level simulated PSD of the 2nd-order CT LPSDM.



(a) (b)

Figure 6.17. Layouts of the 2nd-order CT LPSDM. (a) stand-along chip; (b) modulator core.

6.6 Summary

The development of a 1 GHz second-order CT LPSDM is presented from the system level analysis down to the circuit level design.

The trade-off between the quantiser speed limitation and the access delay is analysed in detail. The NRZ DAC pulse is chosen to relax the challenging design of an ultra fast quantiser. A delayed NTF is synthesised to compensate for the unit clock delay in the quantiser.

Instead of a conventional $G_m - C$ integrator, a lossy integrator with resistive loads were employed because of its small parasitic capacitance at the integrator output nodes, so that the integrator transfer function can be realised at high frequencies. The leaked current through the resistance loads is compensated for by a negative transconductor, and hence a high DC gain is obtained.

A modified master-slave comparator is designed to favour the low voltage application. The trade-off between the quantiser sensitivity and speed is solved by cascading three stages of the master-slave comparators, but introducing a unit clock delay, which is compensated for in the loop filter.

The transistor level SPICE simulation shows that the modulator is capable for the IEEE802.11a WLAN analog-to-digital conversion, and consumes 80 mW power.

Chapter 7

Summary and Future Work

7.1 Summary

Wireless communication technologies are no longer limited for voice band applications, but have entered the era for multimedia data link. The IEEE802.11 family specifies the standards for wireless LAN applications, which occupy the bandwidth at the multi-mega hertz region. The broadband nature of the wireless applications allow the use of the direct downconversion architecture because the receiver impairments at low frequencies can be reduced to an acceptable level.

This thesis described the design of a direct downconversion receiver for the IEEE802.11a specification, including the frontend, baseband processing circuitry, and the SDM ADC.

Chapter 1 provided the project motivation for developing a monolithic receiver solution for the IEEE802.11a specification.

Chapter 2 discussed pros and cons of typical receiver architectures, including the heterodyne, image-rejection heterodyne, low-IF, and the direct downconversion types. The low frequency non-idealities in a direct downconversion receiver, which limited the implementation in the last a few decades, were highlighted. The reasons of using the direct down conversion architecture for the modern broadband receivers were explained.

Chapter 3 was focused on the IEEE802.11a specification, further discussing the advantage of using direct downconversion architecture for the OFDM modulation. The

required receiver noise figure, gain, and the linearity were analysed according to the specification. An IEEE802.11a physical link SIMULINK model was setup for the system level receiver simulations, including the impairments of the thermal, flicker noise, phase noise, and the quadrature mismatches. The fundamental of pulse shaping and the method of creating the flicker noise in SIMULINK were also introduced.

The circuit level analysis and design were presented in Chapter 4. The LNA design methodology using CMOS process was first introduced. With an extra gate capacitance, very low noise figure and low power dissipation were obtained in the practical design. The mixer conversion gain with sinusoidal LO signals was calculated, and also multi-mechanisms of the flicker noise presented at the mixer output were analysed in detail. Some circuit level techniques to reduce the flicker noise feedthrough were introduced. The mixer and VGA interface using capacitance coupling was employed for the best noise performance. The coupling capacitors were re-used for the highpass filter to remove the DC offset, saving the silicon area. The frontend and two VGA stages provide total 42∼90 dB adjustable voltage gain with 1 dB step controlled by the AGC unit. The total sixth-order channel-selection filter was combined by a second-order Butterworth LPF and a fourth-order Chebyshev II LPF, selecting the 9 MHz baseband.

Chapter 5 introduced the fundamentals of the Sigma-Delta modulator for the baseband signal analog-to-digital conversion. A fast synthesis methodology of NTF using MATLAB was developed. The SDM simulations using state-space technique and SIMULINK were described. The algorithm and the circuit topology of a variable centre frequency BPSDM were developed for digital downconversion receivers. The centre frequency can be chosen from very low up to about a half of the sampling frequency and maintain the modulator stability. The continuous-time SDM design methodology with an NRZ or an RZ DAC was discussed.

In chapter 6, a novel 1 GHz LPSDM using TSMC 0.18µm CMOS process was presented. The access loop delay effect in a CT SDM was first examined. The NRZ DAC was chosen for the ultra fast CT SDM to relax the challenge of the high speed quantiser design. A lossy integrator with a negative transconductance compensation realises the transfer function at the high frequencies. A three-stage comparator compromises the sensitivity and speed, however introducing a unity delay, which is compensated for in the loop filter. The circuit level simulation shows a graceful noise shaping due to the accurate control of

the transconductance elements. The second-order modulator achieves 62 dB SNR with a 9 MHz bandwidth and consumes 80 mW of power.

The receiver design including the frontend and baseband circuitry reveals that the direct downconversion architecture, implemented in 0.18 µm CMOS technology, is suitable for the IEEE802.11a standard. Also the deep submicron CMOS process is capable for a broadband analog-to-digital conversion based on the results of the SDM design. Unfortunately due to the funding issue, the final chip couldn't be fabricated for measurement. However, all the circuit level simulations using the foundry models and HSPICE or ADS2003 simulators provide an accurate estimation of the performance.

7.2 Future Work

Device evaluations by fabrication and measurement are crucial in the microelectronics area. So that if there is a chance in the future for the chip fabrication, it should be the first future work to do; especially to test the CMOS LNA by the (I_{ds}, Q_{in}) design methodology, the variable centre frequency BPSDM and the 1 GHz CT LPSDM.

Monolithic receiver-DSP SOC chips bring great convenience for system developers. The challenge to achieve the SOC target is to integrate the RF, analog and DSP function units on a single chip, while avoiding the substrate noise coupling. This challenge leads to the research area of the chip level noise coupling model via the silicon substrate, effective isolation techniques, and the proper clock selection for the digital processing circuitry.

Multi-stand receiver chips, such as IEEE802.11a/b/g and CDMA 3G combinations, are promising for system integrations. Therefore, there is a challenge for the design of RF microelectronics, which are able to accommodate multi-specifications with acceptable power consumptions. Concurrent LNA, matching the impedance at different frequencies, has been reported in the literature [68]. However, the improvement of the LNA noise matching at different radio frequencies maybe worth to investigate in the future.

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Appendix A

AMI 1.5µm CMOS Spice Models for the VCFBPSDM Design

*** AMI 1.5um CMOS Model TT ***

.MODEL CMOSN NMOS (LEVEL = 49 VERSION = 3.1 TNOM = 27 TOX = 3.09E-8 XJ = 3E-7 NCH = 7.5E16 VTH0 = 0.5585921 K1 = 0.9300373 K2 = -0.0706188 K3 = 8.0262635 K3B = -2.4231517 W0 = 5.489201E-7 NLX = 1E-8 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 0.7666071 DVT1 = 0.2843554 DVT2 = -0.2195483 U0 = 665.4919858 UA = 1.468437E-9 UB = 1.94634E-18 UC = 3.408801E-11 VSAT = 1.059876E5 A0 = 0.560251 AGS = 0.1065613 B0 = 2.451371E-6 B1 = 5E-6 KETA = -7.033813E-3 A1 = 0 A2 = 1 RDSW = 3E3 PRWG = -0.0415097 PRWB = -0.0367395 WR = 1 WINT = 7.154435E-7 LINT = 2.218865E-7 XL = 0 XW = 0 DWG = -1.936445E-8 DWB = 3.48297E-8 VOFF = -0.0307548 NFACTOR = 0.5740385 CIT = 0 CDSC = 0 CDSCD = 0 CDSCB = 3.251492E-5 ETA0 = -1 ETAB = -0.5546384 DSUB = 1 PCLM = 1.2454756 PDIBLC1 = 8.119599E-3 PDIBLC2 = 1.824339E-3 PDIBLCB = -0.1 DROUT = 0.0536917 PSCBE1 = 2.410329E9 PSCBE2 = 1.306019E-9 PVAG = 0.149629 DELTA = 0.01 RSH = 52.2 MOBMOD = 1 PRT = 182.01 UTE = -1.5 KT1 = -0.282143 KT1L = 3.296E-9 KT2 = 0 UA1 = 1.206664E-9 UB1 = -5.06439E-18 UC1 = -1E-10 AT = 1E5 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 1.8E-10 CGSO = 1.8E-10 CGBO = 1E-9 CJ = 2.830976E-4 PB = 0.99 MJ = 0.537762 CJSW = 1.451536E-10 PBSW = 0.99 MJSW = 0.1 CJSWG = 6.4E-11 PBSWG = 0.99 MJSWG = 0.1 CF = 0 AF = 1 KF = 0) *

.MODEL CMOSP PMOS (LEVEL = 49 VERSION = 3.1 TNOM = 27 TOX = 3.09E-8 XJ = 3E-7 NCH = 2.4E16 VTH0 = -0.8476404 K1 = 0.4513608 K2 = 2.379699E-5 K3 = 13.3278347 K3B = -2.2238332 W0 = 9.577236E-7 NLX = 1E-8 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 0.2478839 DVT1 = 0.1169086 DVT2 = -0.5 U0 = 236.8923827 UA = 3.833306E-9 UB = 1.487688E-21 UC = -1.08562E-10 VSAT = 1.019808E5 A0 = 0.3104634 AGS = 0.4374691 B0 = 3.217752E-6 B1 = 4.959246E-6 KETA = -0.0196746 A1 = 0 A2 = 0.364 RDSW = 3E3 PRWG = 0.1198926 PRWB = -0.2481551 WR = 1 WINT = 7.565065E-7 LINT = 9.161352E-8 XL = 0 XW = 0 DWG = -2.13917E-8 DWB = 3.857544E-8 VOFF = -0.0877184 NFACTOR = 0.2508342 CIT = 0 CDSC = 2.924806E-5 CDSCD = 1.497572E-4 CDSCB = 1.091488E-4 ETA0 = 0.18903 ETAB = -3.128292E-3 DSUB = 0.2873 PCLM = 3.9336407 PDIBLC1 = 1.935475E-5 PDIBLC2 = 1.308368E-3 PDIBLCB = -1E-3 DROUT = 8.135421E-3 PSCBE1 = 3.351476E9 PSCBE2 = 5.018187E-10 PVAG = 15 DELTA = 0.01 RSH = 75.6 MOBMOD = 1 PRT = 246.403 UTE = -1.5 KT1 = -0.6104394 KT1L = 3.372457E-8 KT2 = 0 UA1 = -1.127018E-9 UB1 = 1.95240E-18 UC1 = -1E-10 AT = 1E5 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 2.26E-10 CGSO = 2.26E-10 CGBO = 1E-9 CJ = 2.750013E-4 PB = 0.7304623 MJ = 0.4163053 CJSW = 1.667296E-10 PBSW = 0.99 MJSW = 0.1387033 CJSWG = 3.9E-11 PBSWG = 0.99 MJSWG = 0.1387033 CF = 0 AF = 1 KF = 0) *

*** AMI 1.5um CMOS Model FF ***

.MODEL CMOSN NMOS (LEVEL = 49 VERSION = 3.1 TNOM = 27 TOX = 3.09E-8 XJ = 1.5E-7 NCH = 1.7E17 VTH0 = 0.3418879 K1 = 1 K2 = -0.0886142 K3 = 73.935439 K3B = -1.7335131 W0 = 4.294837E-6 NLX = 1.234757E-7 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 0.9366704 DVT1 = 0.3952099 DVT2 = -0.5 U0 = 512.1053322 UA = 1E-13 UB = 3.542293E-21 UC = -2.6555E-11 VSAT = 1.262501E5 A0 = 0.6976947 AGS = 0.1141915 B0 = 1.665024E-6 B1 = 5E-6 KETA = 1.004654E-3 A1 = 4.087651E-3 A2 = 0.4749696 RDSW = 2.240384E3 PRWG = 0.0865258 PRWB = 0.1022712 WR = 1 WINT = 3.502972E-7 LINT = 2.66482E-7 XL = 0 XW = 0 DWG = 8.182647E-8 DWB = 1E-7 VOFF = 0 NFACTOR = 0 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0 ETA0 = 4.931902E-3 ETAB = -2.258513E-3 DSUB = 0.0881464 PCLM = 2.9105077 PDIBLC1 = 1.5770646 PDIBLC2 = 2.55284E-3 PDIBLCB = -0.0422318 DROUT = 2 PSCBE1 = 2.446215E8 PSCBE2 = 1.803554E-6 PVAG = 0 DELTA = 0.01 RSH = 52.9 MOBMOD = 1 PRT = 182.01 UTE = -1.5 KT1 = -0.282143 KT1L = 3.296E-9 KT2 = 0 UA1 = 1.206664E-9 UB1 = -5.06439E-18 UC1 = -1E-10 AT = 1E5 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 1.79E-10 CGSO = 1.79E-10 CGBO = 1E-10 CJ = 2.819907E-4 PB = 0.9892543 MJ = 0.5329971 CJSW = 1.60816E-10 PBSW = 0.2095614 MJSW = 0.1 CJSWG = 6.4E-11 PBSWG = 0.2095614 MJSWG = 0.1 CF = 0 AF = 1 KF = 0)

.MODEL CMOSP PMOS (LEVEL = 49 VERSION = 3.1 TNOM = 27 TOX = 3.09E-8 XJ = 1.5E-7 NCH = 1.7E17 VTH0 = -0.5412091 K1 = 0.4956702 K2 = -0.0172116 K3 = 29.1047334 K3B = -0.349145 W0 = 6.643926E-7 NLX = 9.869849E-7 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 1.2567763 DVT1 = 0.1934763 DVT2 = -0.1101939 U0 = 213.8783744 UA = 2.609406E-9 UB = 2.126194E-19 UC = -9.91697E-11 VSAT = 2E5 A0 = 1.0812191 AGS = 0.2151663 B0 = 3.026533E-6 B1 = 5E-6 KETA = -4.041454E-4 A1 = 0 A2 = 0.3 RDSW = 3E3 PRWG = 0.1606075 PRWB = 0.026623 WR = 1 WINT = 5E-7 LINT = 1.070949E-7 XL = 0 XW = 0 DWG = 5.26422E-8 DWB = 1E-7 VOFF = -6.706867E-3 NFACTOR = 0.1930646 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0 ETA0 = 1 ETAB = 0.422708 DSUB = 0.7758321 PCLM = 10 PDIBLC1 = 0.5648689 PDIBLC2 = 0 PDIBLCB = 5.712687E-3 DROUT = 0.2362627 PSCBE1 = 1E8 PSCBE2 = 5E-10 PVAG

= 7.4222093 DELTA = 0.01 RSH = 75.5 MOBMOD = 1 PRT = 246.403 UTE = -1.5 KT1 = -0.6104394 KT1L = 3.372457E-8 KT2 = 0 UA1 = -1.127018E-9 UB1 = 1.952401E-18 UC1 = -1E-10 AT = 1E5 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 2.26E-10 CGSO = 2.26E-10 CGBO = 1E-10 CJ = 2.750024E-4 PB = 0.7311843 MJ = 0.4165128 CJSW = 1.665418E-10 PBSW = 0.9889114 MJSW = 0.1377668 CJSWG = 3.9E-11 PBSWG = 0.9889114 MJSWG = 0.1377668 CF = 0 AF = 1 KF = 0) *

*** AMI 1.5um CMOS Model SS ***

.MODEL CMOSN NMOS (LEVEL = 49 VERSION = 3.1 TNOM = 27 TOX = 3.1E-8 XJ = 3E-7 NCH = 7.5E16 VTH0 = 0.5938928 K1 = 0.9606589 K2 = -0.0722108 K3 = 8.0613938 K3B = -2.5714751 W0 = 1.259046E-6 NLX = 1E-8 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 0.7298898 DVT1 = 0.3187254 DVT2 = -0.2774341 U0 = 673.9743329 UA = 1.655142E-9 UB = 1.736126E-18 UC = 4.035809E-11 VSAT = 1.083534E5 A0 = 0.4962064 AGS = 0.0873111 B0 = 2.346374E-6 B1 = 5E-6 KETA = -0.0107375 A1 = 0 A2 = 1 RDSW = 3E3 PRWG = -0.0324038 PRWB = -0.0446512 WR = 1 WINT = 7.242762E-7 LINT = 2.231816E-7 XL = 0 XW = 0 DWG = -2.638688E-8 DWB = 3.30262E-8 VOFF = -0.0424245 NFACTOR = 0.6653555 CIT = 0 CDSC = 0 CDSCD = 0 CDSCB = 4.394359E-5 ETA0 = -1 ETAB = -0.5939699 DSUB = 0.9988851 PCLM = 1.2994807 PDIBLC1 = 8.97257E-3 PDIBLC2 = 1.811508E-3 PDIBLCB = -0.1 DROUT = 0.0581877 PSCBE1 = 1E8 PSCBE2 = 5.480445E-10 PVAG = 0.3163861 DELTA = 0.01 RSH = 54.2 MOBMOD = 1 PRT = 182.01 UTE = -1.5 KT1 = -0.282143 KT1L = 3.296E-9 KT2 = 0 UA1 = 1.206664E-9 UB1 = -5.06439E-18 UC1 = -1E-10 AT = 1E5 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 1.78E-10 CGSO = 1.78E-10 CGBO = 1E-9 CJ = 2.831147E-4 PB = 0.9892624 MJ = 0.5375655 CJSW = 1.448993E-10 PBSW = 0.9892613 MJSW = 0.1 CJSWG = 6.4E-11 PBSWG = 0.9892613 MJSWG = 0.1 CF = 0 AF = 1 KF = 0) *

.MODEL CMOSP PMOS (LEVEL = 49 VERSION = 3.1 TNOM = 27 TOX = 3.1E-8 XJ = 3E-7 NCH = 2.4E16 VTH0 = -0.8476404 K1 = 0.4513608 K2 = 2.379699E-5 K3 = 13.3278347 K3B = -2.2238332 W0 = 9.577236E-7 NLX = 4.413182E-7 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 0.9351981 DVT1 = 1 DVT2 = -0.3102606 U0 = 236.8923827 UA = 3.833306E-9 UB = 1.487688E-21 UC = -1.08562E-10 VSAT = 1.479579E5 A0 = 0.3545329 AGS = 0.0598437 B0 = 3.370831E-6 B1 = 5E-6 KETA = -2.815104E-3 A1 = 0 A2 = 0.364 RDSW = 3E3 PRWG = 0.0510944 PRWB = -0.2978596 WR = 1 WINT = 7.565065E-7 LINT = 3.915524E-8 XL = 0 XW = 0 DWG = -2.13917E-8 DWB = 3.857544E-8 VOFF = -0.0877184 NFACTOR = 0.2508342 CIT = 0 CDSC = 2.924806E-5 CDSCD = 1.497572E-4 CDSCB = 1.091488E-4 ETA0 = 0.18903 ETAB = -3.126169E-3 DSUB = 0.2873 PCLM = 3.6298983 PDIBLC1 = 3.071687E-6 PDIBLC2 = 1.029847E-3 PDIBLCB = -9.979309E-4 DROUT = 5.642687E-4 PSCBE1 = 3.348257E9 PSCBE2 = 5.013367E-10 PVAG = 14.9962419 DELTA = 0.01 RSH = 76.9 MOBMOD = 1 PRT = 246.403 UTE = -1.5 KT1 = -0.6104394 KT1L = 3.372457E-8 KT2 = 0 UA1 = -1.127018E-9 UB1 = 1.952401E-18 UC1 = -1E-10 AT = 1E5 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 2.18E-10 CGSO = 2.18E-10 CGBO = 1E-9 CJ = 2.750004E-4 PB = 0.7304697 MJ = 0.4163034 CJSW = 1.667377E-10 PBSW = 0.9891238 MJSW = 0.138695 CJSWG = 3.9E-11 PBSWG = 0.9891238 MJSWG = 0.138695 CF = 0 AF = 1 KF = 0) *

*** AMI 1.5um CMOS Model FS ***

.MODEL CMOSN NMOS (LEVEL = 49 VERSION = 3.1 TNOM = 27 TOX = 3.1E-8 XJ = 1.5E-7 NCH = 1.7E17 VTH0 = 0.3552941 K1 = 1 K2 = -0.0902551 K3 = 80.4408341 K3B = -2.0401761 W0 = 5.986863E-6 NLX = 2.004975E-7 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 1.1516023 DVT1 = 0.3035573 DVT2 = -0.2699118 U0 = 525.7080358 UA = 1E-13 UB = 2.178146E-20 UC = -4.24067E-11 VSAT = 1.330286E5 A0 = 0.6608039 AGS = 0.0739246 B0 = 1.234506E-6 B1 = 5E-6 KETA = 6.152135E-4 A1 = 0.0319649 A2 = 0.3555416 RDSW = 2.776237E3 PRWG = 0.0434954 PRWB = 0.0513048 WR = 1 WINT = 3.615794E-7 LINT = 2.824851E-7 XL = 0 XW = 0 DWG = 7.804304E-8 DWB = 1E-7 VOFF = 0 NFACTOR = 0 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0 ETA0 = 3.988663E-3 ETAB = -1.860237E-3 DSUB = 0.0717376 PCLM = 2.9673455 PDIBLC1 = 1.7324734 PDIBLC2 = 2.44682E-3 PDIBLCB = -0.0311057 DROUT = 1.3514359 PSCBE1 = 1.980083E8 PSCBE2 = 5.517543E-7 PVAG = 0 DELTA = 0.01 RSH = 54.7 MOBMOD = 1 PRT = 182.01 UTE = -1.5 KT1 = -0.282143 KT1L = 3.296E-9 KT2 = 0 UA1 = 1.206664E-9 UB1 = -5.06439E-18 UC1 = -1E-10 AT = 1E5 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 1.79E-10 CGSO = 1.79E-10 CGBO = 1E-10 CJ = 2.819905E-4 PB = 0.9892687 MJ = 0.5330165 CJSW = 1.608294E-10 PBSW = 0.2096834 MJSW = 0.1 CJSWG = 6.4E-11 PBSWG = 0.2096834 MJSWG = 0.1 CF = 0 AF = 1 KF = 0) *

.MODEL CMOSP PMOS (LEVEL = 49 VERSION = 3.1 TNOM = 27 TOX = 3.1E-8 XJ = 1.5E-7 NCH = 1.7E17 VTH0 = -0.8238582 K1 = 0.4609855 K2 = -4.53208E-4 K3 = 24.9924178 K3B = -1.2223282 W0 = 1.209388E-6 NLX = 1E-6 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 1.4457275 DVT1 = 0.1964752 DVT2 = -0.0651827 U0 = 225.374352 UA = 3.222769E-9 UB = 3.845902E-19 UC = -8.36683E-11 VSAT = 2E5 A0 = 0.1463702 AGS = 0.0112579 B0 = 4.487759E-6 B1 = 5E-6 KETA = -7.612061E-3 A1 = 0 A2 = 0.3 RDSW = 3E3 PRWG = 0.1220022 PRWB = -0.0602275 WR = 1 WINT = 5E-7 LINT = 8.641214E-8 XL = 0 XW = 0 DWG = 5.360576E-8 DWB = 1E-7 VOFF = -0.0329443 NFACTOR = 0.1439157 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0 ETA0 = 0.4151491 ETAB = -0.0627808 DSUB = 0.3810547 PCLM = 10 PDIBLC1 = 1.236252E-3 PDIBLC2 = 1.178347E-3 PDIBLCB = -0.1 DROUT = 0 PSCBE1 = 1E8 PSCBE2 = 8.935016E-10 PVAG = 15 DELTA = 0.01 RSH = 76.1 MOBMOD = 1 PRT = 246.403 UTE = -1.5 KT1 = -0.6104394 KT1L = 3.372457E-8 KT2 = 0 UA1 = -1.127018E-9 UB1 = 1.952401E-18 UC1 = -1E-10 AT = 1E5 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 2.23E-10 CGSO = 2.23E-10 CGBO = 1E-10 CJ = 2.750024E-4 PB = 0.7311609 MJ = 0.4165067 CJSW = 1.665496E-10 PBSW = 0.9888326 MJSW = 0.1377907 CJSWG = 3.9E-11 PBSWG = 0.9888326 MJSWG = 0.1377907 CF = 0 AF = 1 KF = 0) *

*** AMI 1.5um CMOS Model SF ***

.MODEL CMOSN NMOS (LEVEL = 49 VERSION = 3.1 TNOM = 27 TOX = 3.1E-8 XJ = 1.5E-7 NCH = 1.7E17 VTH0 = 0.4614515 K1 = 1 K2 = -0.0705094 K3 = 68.5120173 K3B = -1.6803968 W0 = 4.639473E-6 NLX = 1.585868E-7 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 1.0455678 DVT1 = 0.354009 DVT2 = -0.3737356 U0 = 520.9170195 UA = 1.765927E-12 UB = 9.213525E-20 UC = -4.60095E-11 VSAT = 1.417942E5 A0 = 0.5127879 AGS = 7.742278E-4 B0 = 1.213886E-6 B1 = 5E-6 KETA = -9.726449E-3 A1 = 0.0285695 A2 = 0.31575 RDSW = 2.817964E3 PRWG = 0.0426905 PRWB = 0.0385776 WR = 1 WINT = 4.015258E-7 LINT = 2.806234E-7 XL = 0 XW = 0 DWG = 7.86338E-8 DWB = 1E-7 VOFF = 0 NFACTOR = 0.0395355 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0 ETA0 = 2.168868E-3

ETAB = -6.298812E-4 DSUB = 0.0291404 PCLM = 2.9949477 PDIBLC1 = 2 PDIBLC2 = 1.045548E-3 PDIBLCB = -0.1985476 DROUT = 1.0985508 PSCBE1 = 1.687442E8 PSCBE2 = 2.05305E-7 PVAG = 0 DELTA = 0.01 RSH = 52.2 MOBMOD = 1 PRT = 182.01 UTE = -1.5 KT1 = -0.282143 KT1L = 3.296E-9 KT2 = 0 UA1 = 1.206664E-9 UB1 = -5.06439E-18 UC1 = -1E-10 AT = 1E5 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 1.78E-10 CGSO = 1.78E-10 CGBO = 1E-10 CJ = 2.819905E-4 PB = 0.9892687 MJ = 0.5330165 CJSW = 1.608294E-10 PBSW = 0.2096834 MJSW = 0.1 CJSWG = 6.4E-11 PBSWG = 0.2096834 MJSWG = 0.1 CF = 0 AF = 1 KF = 0) *

.MODEL CMOSP PMOS (LEVEL = 49 VERSION = 3.1 TNOM = 27 TOX = 3.1E-8 XJ = 1.5E-7 NCH = 1.7E17 VTH0 = -0.7203002 K1 = 0.5028415 K2 = -6.420434E-3 K3 = 25.7018529 K3B = -0.6650859 W0 = 7.616826E-7 NLX = 1E-6 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 1.5853422 DVT1 = 0.2256511 DVT2 = -0.0761088 U0 = 225.9995164 UA = 3.243723E-9 UB = 3.53857E-19 UC = -9.47707E-11 VSAT = 2E5 A0 = 0.5399018 AGS = 0.1772438 B0 = 4.276792E-6 B1 = 5E-6 KETA = -6.330167E-3 A1 = 0 A2 = 0.3 RDSW = 3E3 PRWG = 0.0916148 PRWB = -0.0744168 WR = 1 WINT = 5E-7 LINT = 8.263378E-8 XL = 0 XW = 0 DWG = 6.663649E-8 DWB = 1E-7 VOFF = -0.0375864 NFACTOR = 0.1597389 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0 ETA0 = 0.9459351 ETAB = -0.0941568 DSUB = 0.5462029 PCLM = 10 PDIBLC1 = 0.1715607 PDIBLC2 = 5.132495E-4 PDIBLCB = -0.1 DROUT = 0.1743087 PSCBE1 = 1E8 PSCBE2 = 1.739746E-9 PVAG = 12.4353134 DELTA = 0.01 RSH = 77.4 MOBMOD = 1 PRT = 246.403 UTE = -1.5 KT1 = -0.6104394 KT1L = 3.372457E-8 KT2 = 0 UA1 = -1.127018E-9 UB1 = 1.952401E-18 UC1 = -1E-10 AT = 1E5 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 2.22E-10 CGSO = 2.22E-10 CGBO = 1E-10 CJ = 2.750024E-4 PB = 0.7311609 MJ = 0.4165067 CJSW = 1.665496E-10 PBSW = 0.9888326 MJSW = 0.1377907 CJSWG = 3.9E-11 PBSWG = 0.9888326 MJSWG = 0.1377907 CF = 0 AF = 1 KF = 0) *

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